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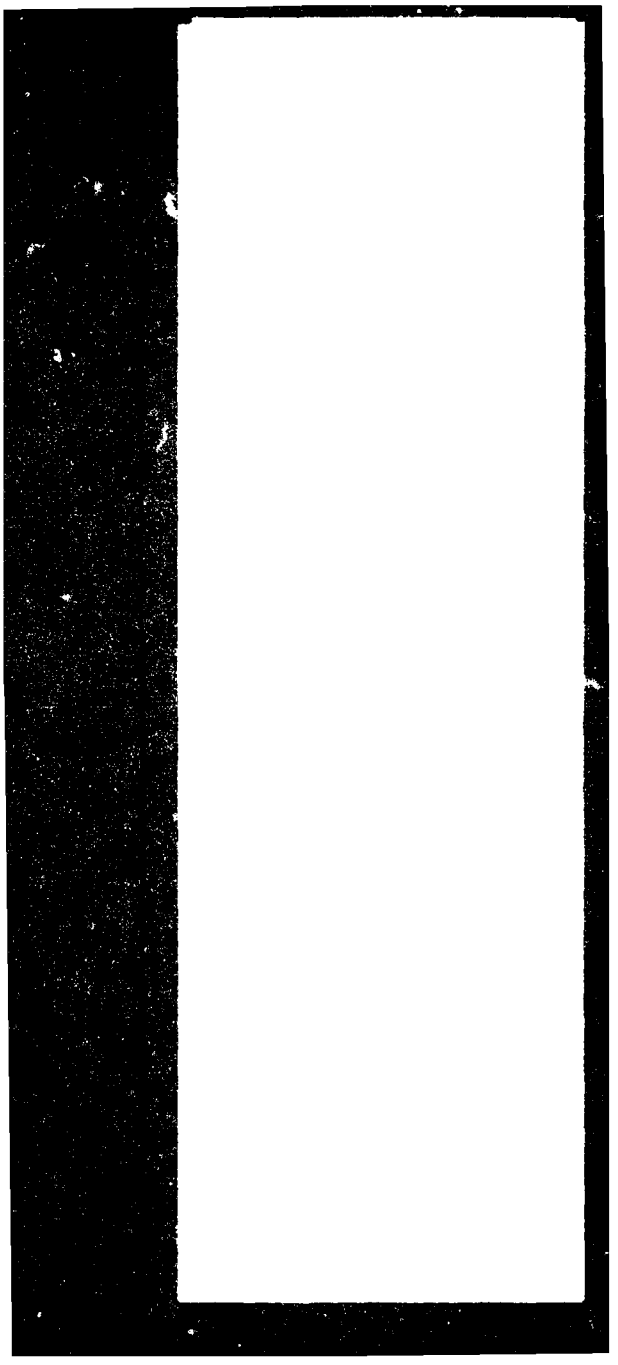

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THE
BENDIX
CORPORATION

Electrodynamics
Division

North Hollywood
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(6) SEA GUARD

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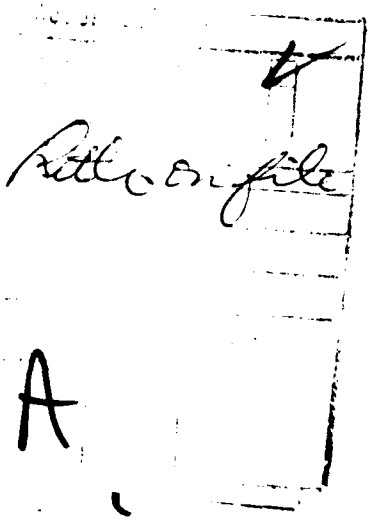
SEA GUARD CONTENTS

I. INTRODUCTION

This Report documents the results of a study performed by Bendix Electrodynamics Division to develop the data multiplex subsystem for a moored acoustic sensing system utilizing the "Thin Line Telemetry System" presently under development for NUSC/NL. The moor acoustic sensing system, identified as the "Seaguard System," is similar technically and physically to the Thin Line Array (TLA) and can use TLA hardware with a minimum of changes. The major difference is due to the greatly increased transmission distances required by Seaguard and the problems of testing and maintaining such a long array once it has been deployed.

This report is both a direct reply to the "Task Statement for the Seaguard Multiplex System," (NUSC/NL-SA14:LFD:ljw-3900-Ser SA14-46-25 March 1975) and a general evaluation of the system requirements. Therefore, three types of heading designations are used. The Roman numeral designations contained in the Table of Contents refer to the report partitioning of the problem into common subject matter. The number designations referred to in the various sections are taken directly from the NUSC/NL task statement. The alphabetic designations are used to summarize various trade offs in system architecture.



II. SUMMARY

This section is a tabular summary of the results of the study.

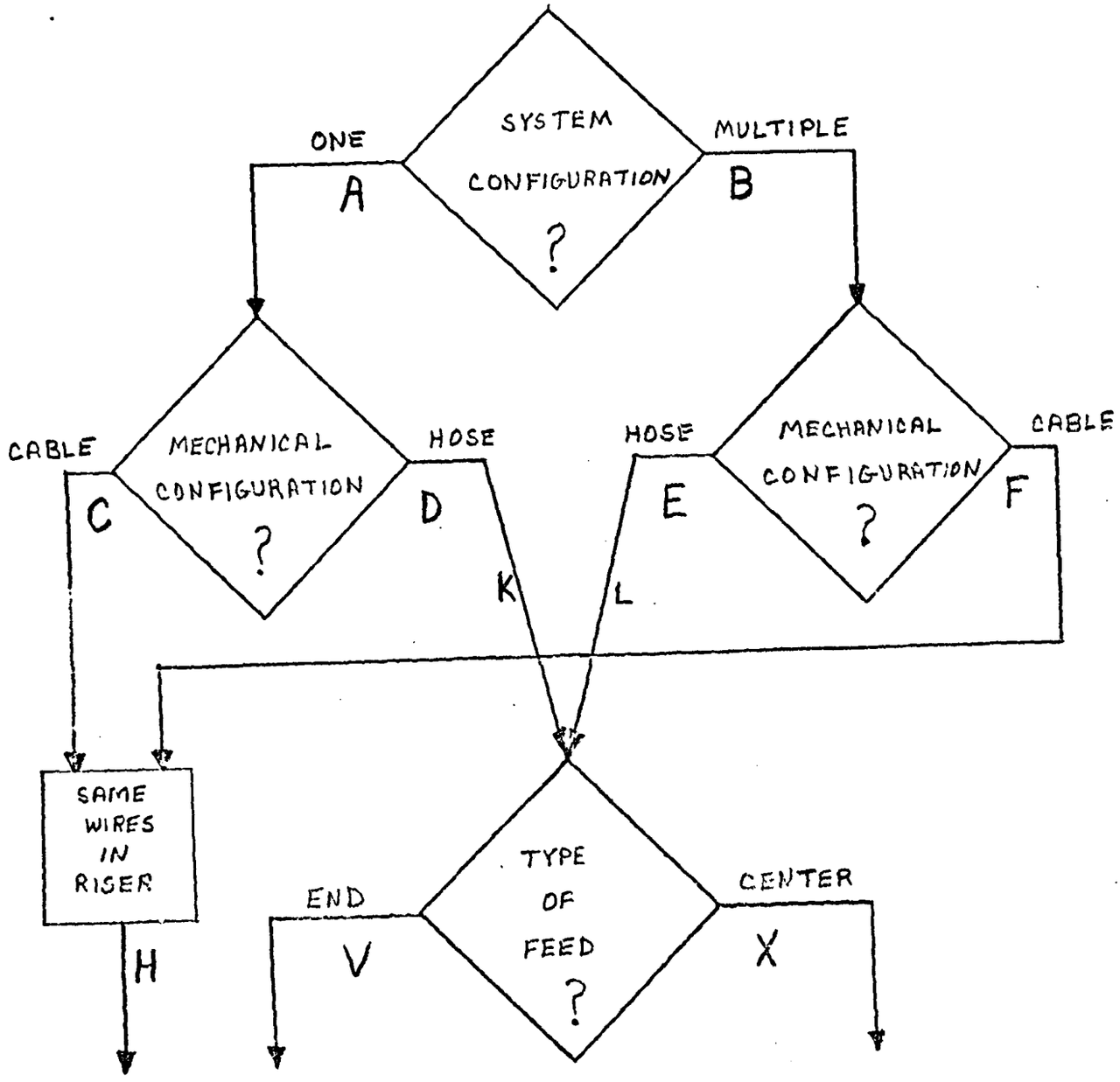
II-a. SUMMARY OF POWER DISTRIBUTION METHODS

There are six possible configurations that need investigation. These are the six paths shown in the Flow Diagram and the Summary Table.

Using an end-fed series power distribution is not practical because of the high voltage gradients which would exist along the array.

Using a center-fed series power distribution reduces the voltages but requires large conductor sizes and would require voltage limiting to prevent over-voltage in case of partial failure.

Any of the parallel power distribution methods could be used. It is recommended that the configuration of Figure 6 be used if a hose is used to contain the conductors and that the configuration of Figure B-4 be used if a continuous cable is used for the conductors.



POWER TRANSMISSION METHODS

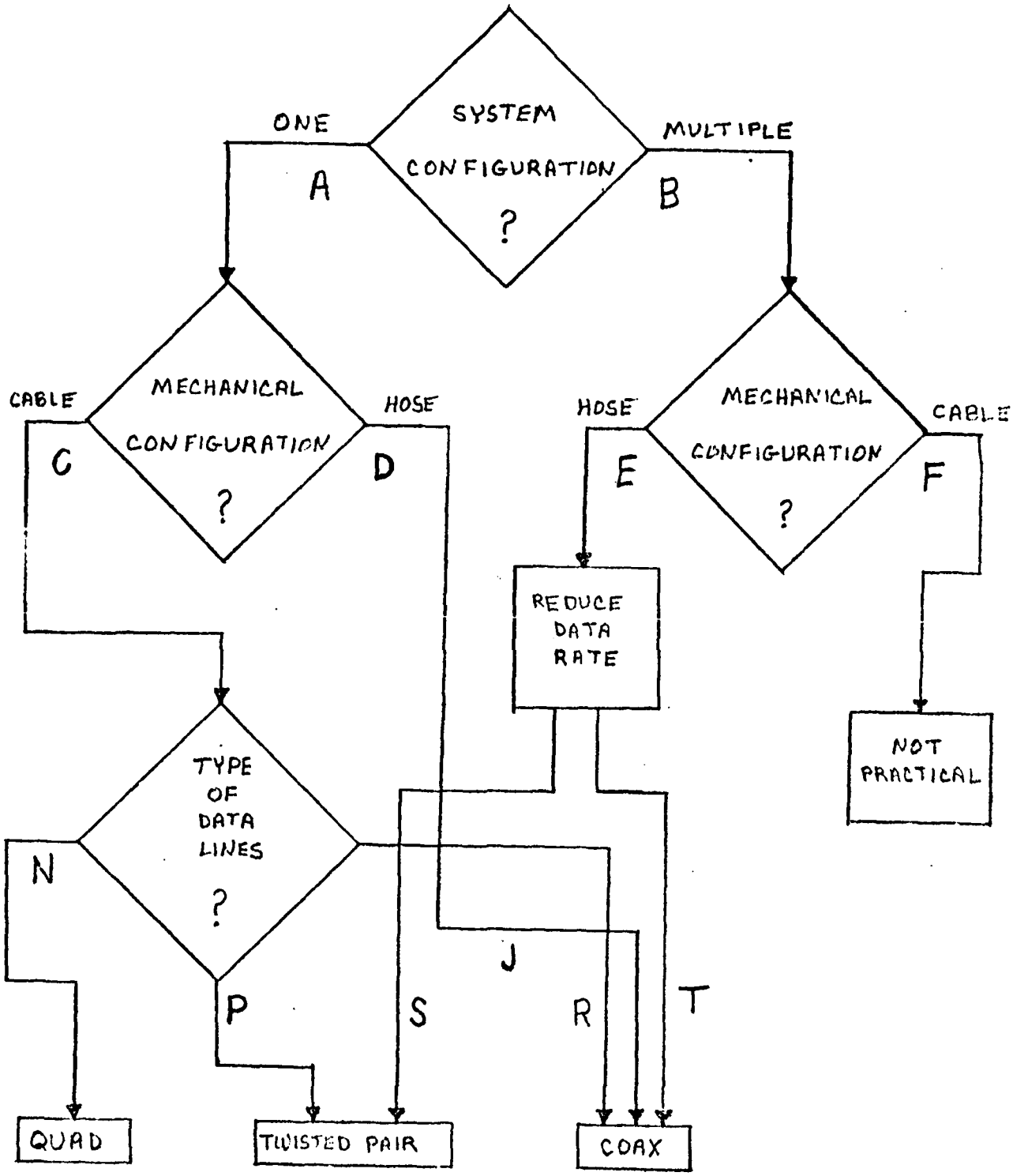
FIGURE II-a

CONFIGURATION	WIRE QTY - SIZE	WEIGHT ARRAY & RISER	REF. DWG.	COMMENTS
ACH	NOT DONE BUT WILL BE WORSE THAN ADKV			
ADKV	ARRAY: 4-18 RISER: 4-12	1493 lbs	FIG. A3, A6	NOT USE FUL BECAUSE OF HIGH VOLTAGE DIFFERENCES
ADKX	ARRAY: 4-18 RISER: 2-12	1488 lbs	FIG A10	
BELV	ARRAY: 8-18 RISER: 2-18 2-14 4-12	2543 lbs	FIG. 5	
	ARRAY: 8-18 RISER: 2-18 4-16 2-12	2202 lbs	FIG. 6	RECOMMENDED SYSTEM
	4-14, 4-12	3586 lbs	FIG B1	
	6-14, 2-12	4052 lbs	FIG. B2	
BELX	ARRAY: 4-18 RISER: 4-12	2380 lbs	FIG. A2, A5	
BFH	2-18, 4-16, 2-14	2578 lbs	FIG B4	ALTERNATE RECOMMENDED SYSTEM

SUMMARY

POWER TRANSMISSION METHODS

TABLE II-a



DATA TRANSMISSION METHODS

FIGURE II-b

II-b. SUMMARY

FLOW	NO. OF RE-PEATERS	RE-PEATER SPACING	CLOCK & DATA CABLE TYPE	CABLE DIA. X NO. OF CABLES	ARRAY CABLE WEIGHT	RISER CABLE WEIGHT	TOTAL CABLE WEIGHT
ACN* 6.1 (4)							
ACP 6.2.3(a)	11	1818'	AWG 15 SH.TW.PR	.344 (2)	3200	800	4000
ACR 6.2.3(a)	9	2222'	RG54A Coax	.250 (2)	1460	730	2190
ADJ 6.2.3(a)	9	2222'	RG54A Coax	.250 (2)	1460	730	2190
BES 6.2.3(b)	9	2222'	AWG 19 SH.TW.PR	.212 (2-5)	1890	1350	3240
BET 6.2.3(b)	6	3333'	RG122 COAX	.160 (2-5)	1120	800	1920

*Requires modification of transmitters for balanced input and output.

II-c. SUMMARY - FORMAT TRADEOFFS

CLOCK FREQ.	DATA BW	# OF ADDR	Δ SIZE	Δ POWER	# OF SUBSTRATES AFFECTED	REMARKS
6 mHz	1000 Hz	256	0 SQ IN	0	None	TLA
6	500	512	.05	0	2	50% blanks
3	1000	128	.06	-.1W	4	2 sub-arrays
3	500	256	.11	-.1W	4	
1.5	1000	64	.18	-.15W	4	4 sub-arrays
1.5	500	128	.23	-.15W	5	2 sub-arrays

COHERENT CALIBRATION SOURCE TRADE-OFFS

METHOD	POWER	SIZE	SPECTRUM	EXP. AMPL. DRIFT
PRN Fltr'd	+.01W	.012 SQ IN	Good	2%
PRN-DAC	+.03W	.023	Best	½%
Sawtooth	+.03W	.034	4th	½%
Triangle	+.03W	.034	3rd	½%
Square Wave	.0002W	.009	5th	½%

II-d. SUMMARY - STATION-CLOCK LINK

NO. OF FREQ.	MODULATION	Δ SIZE	Δ POWER	Remarks
One	Pulse duration	----	---	Single point failure may be difficult to eliminate
One	No. of pulses	.03 SQ IN	0.6 mW	Recommended
Four	---	.25 SQ IN	48 mW	---

CLOCK - TRANSMITTER LINK

PATH	MODULATION	Δ SIZE	Δ POWER	Remarks
Clock Line	Multiple double amp.	.06 SQ IN	1.4 mW	Recommended
Data Line	Status bits	.12 SQ IN	36 mW	Less interchangeability
Twisted Pair	Four tones	.25 SQ IN	48 mW	Add'l hi-voltage capacitors required

II-e. Field Repair

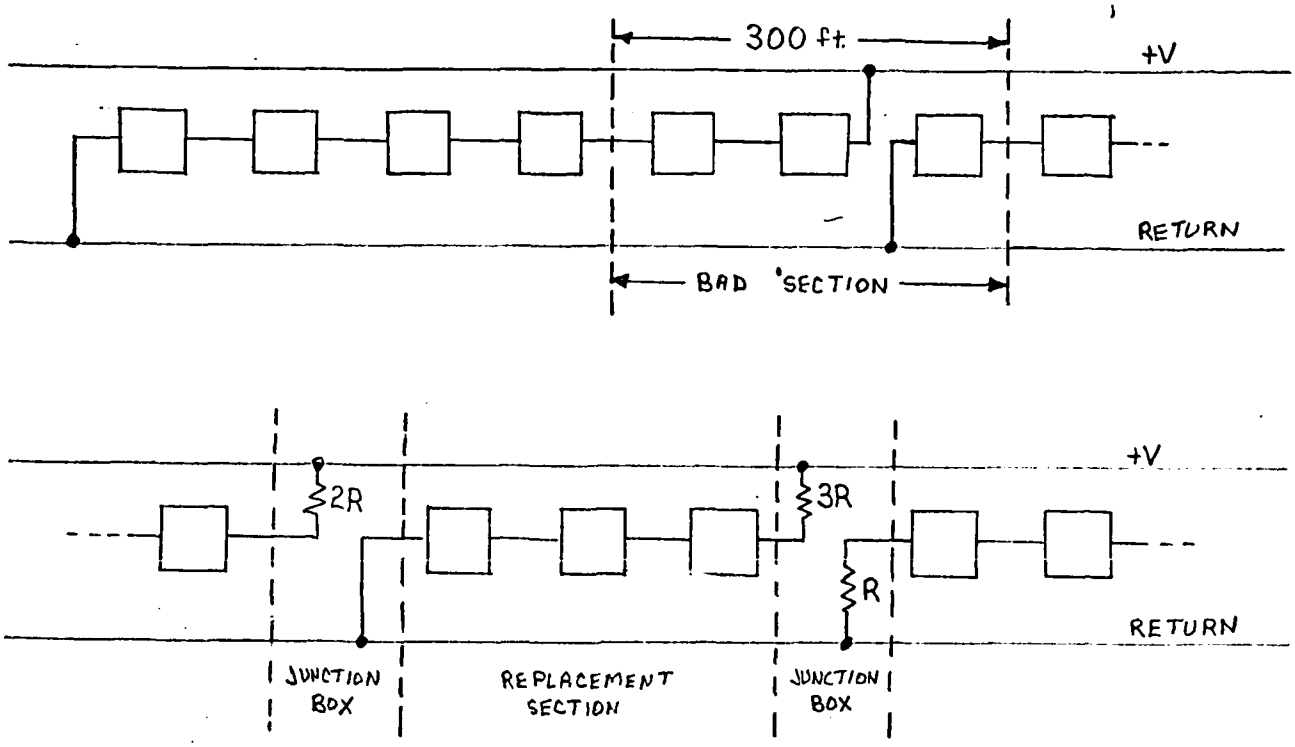
The main problem with field repair is the tapered spacing of the array combined with the tube construction. Of almost equal complexity is the limited number of addresses combined with fixed address transmitter modules. Figure II-e shows the various configurations considered during the study. The results are tabulated in Table II-e.

The cable, if it is field alterable with either an increased address field or header pins allows service at the unit level with a single spare transmitter type (excluding non-acoustic sensors). However, due to the mechanical problems involved in using coaxial cables in a cable system (stretch requirements) the tube system was recommended. (See Section III and V below). The service problem is more complex in the tube system but can be accomplished with the recommended approach (ADK) requiring 5 types of sections and an increased address field. This approach requires an additional flip-flop in the transmitter module and a reduction in input bandwidth which changes the input filter in the transmitter. The bandwidth reduction is a simple ratio problem.

For the suggested bandwidth, the number of total addresses equals 400 exactly.

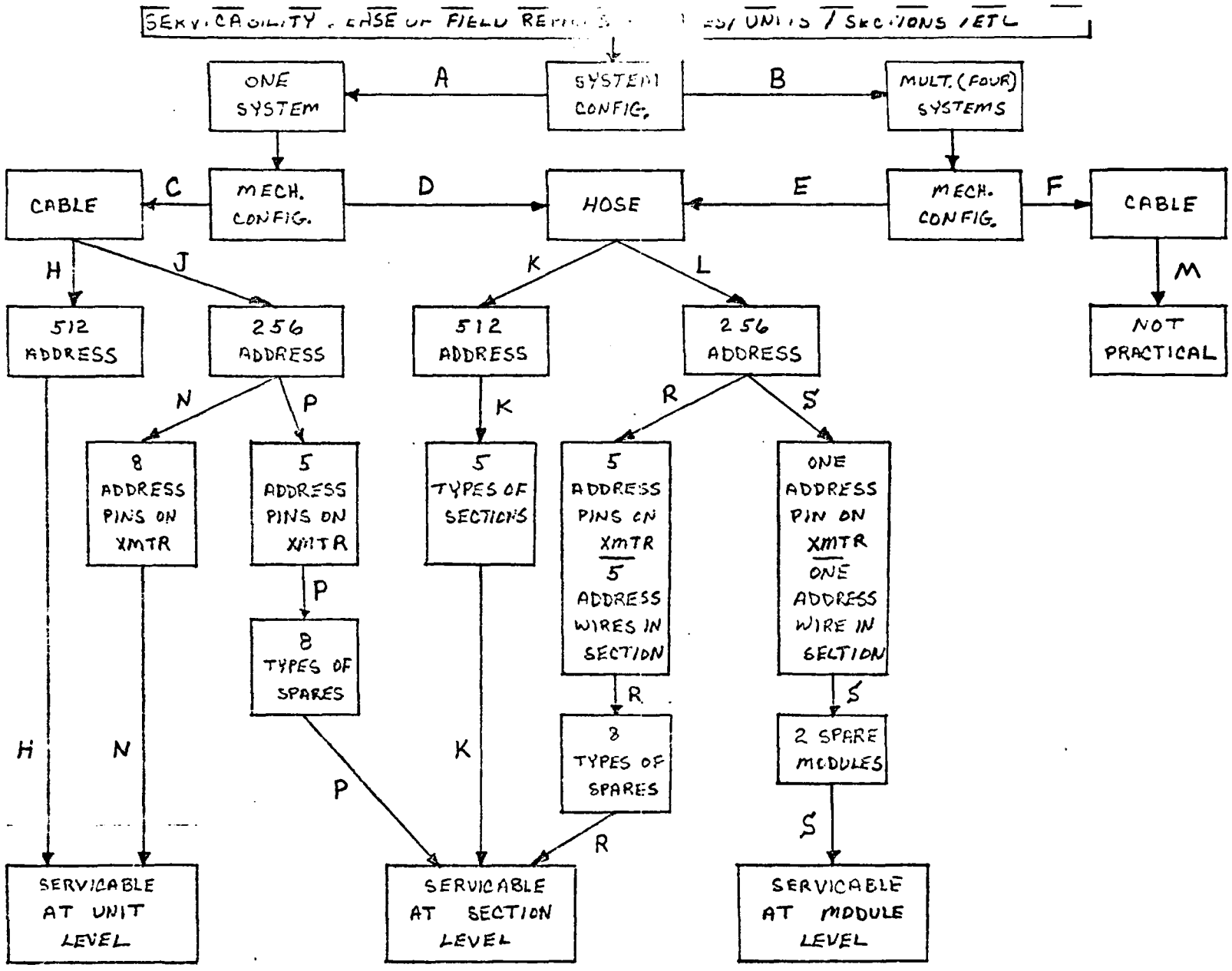
The problem of tapered spacing in the tube requires that there be five different sections, since a 300 foot section may have from 2 to 6 modules

in a section. A further complication is caused by the series power connections for the transmitter modules. The end of a six element string usually ends in the center of a section. This can be circumvented by dummy load resistors as shown below:



The maximum power dissipated by a resistor (a 5R resistor) would be 8.25 watts where R equals the resistor necessary to replace one transmitter

module. The system would see an increased current of 100 milliamperes which in the case of multiple failures corrected by increasing the supply voltage at the receiver.



SEA GUARD SERVICABILITY EVALUATION

FIGURE II-e

TABLE II-e

PATH	NUMBER OF SPARES TYPES	TYPE OF SPARE	ADDT'L PINS ON HEADER	ADDT'L WIRES IN ARRAY
ACH	1	Unit	0	0
ACJN	1	Unit	8	0
ACJP	8	Units	5	0
*ADK	5	Sections	0	0
ADLR	8	Sections	5	5
ADLS	2	Modules	1	1
BELR	8	Sections	5	5
BELS	2	Modules	1	1
B.F.	Not practical - would require 5 coax cables thru cable.			

*Recommended approach.

III. RECOMMENDED SYSTEM

This section is a recommended system for NUSC/NL evaluation. Figure III-a shows the Acid block diagram and recommended interface to the ship and the array riser. DC power, the command signals and data are all transmitted on an RG34B(TRIAX) trunk cable. RG34B is not a triax but with an outer shield will be within the 0.750 constraint. The command, data, and dc power are separated at the "Acid" and sent on separate wires through the array. The riser uses the same wires as the array except for the power wires which uses three wire sizes in the riser and all #18 in the array.

The "Acid" contains a "Clock Generator" and a "Receiver/Inverter" section to invert the transmitted data and force a consistent bit polarity reversal independent of the data source. The data is reversed to provide a ±1 signal on a zero bit and a zero voltage output for a one bit. This reversal of the present system insures a sufficient number of polarity reversals to regenerate the 6 MHz clock at the receiver which eliminates the need for the 6 MHz pilot tone.

The reconstituted data is amplified and driven up the triax trunk cable through an isolating high pass filter by a triply redundant line driver. Each section of the driver supplies 1/3 of the output voltage as a current source into a common terminating resistor. Even if two sections fail the output will drop only 9 dB which is included in the cable evaluation.

The command signal is separated from the data by a low pass filter and amplified by a balanced output amplifier for transmission via a 22 gauge twisted pair to the clock module at the end of the array.

The dc power is "conditioned" at the "Acid" by a 250 watt clamp (5x50W zener diodes) which prevents the voltage from exceeding 242 Vdc. This allows a change of 33 percent in load current without an excessive voltage change on the system. Further protection is provided by smaller zener clamps in the array as will be described below. DC power for the Acid circuits are derived from the 230V line by a dc to dc static inverter. Power for the buffer amplifiers, which are described below, is supplied by a 100 milliampere current source transmitted along the data and clock coax shields. The shields were chosen over the command lines for reliability reasons. The command line is not required for system operation and the shields are required; therefore, using the command lines for the buffer power adds one more series of connections which can cause a system failure.

Figure III-b describes a typical 300 foot section of the tube constructed array. The array is a series of 300 foot sections interconnected by short sections called "Junction Boxes." Most junction boxes are just straight through One-to-One interconnections but at buffer amplifier intervals and at the beginning of each module, there are special active units. The "Power Clamp" junction box allows a zener clamp to be inserted on the power line at the beginning of each module to further protect the circuits against a sudden reduction in load current. It also allows the power distribution system to be modified as best suits each module element as described in Section IV below.

At intervals of 2400 feet a "Clock and Data Buffer" junction box is inserted to compensate for signal loss on the 6 MHz clock line. The data line has less signal loss due to the lower frequency, however, it is

advantagious to use the clock to restrobe the data limiting the signal skew problem to 2400 feet of line. Therefore, the buffer amplifier module amplifies both the clock and the data line. Each amplifier is doubly redundant using current summing as in the Acid power amplifier. If one half the amplifier fails the output will drop 6 dB which is provided for in the transmission loss evaluation.

The 20,000 foot array would have 9 "Buffer Amplifier" junction boxes, 4 "Power Clamp" junction boxes, and a special "Clock" junction box containing the two clock modules. (The main and backup clock modules.) All modules would be identical on pin connections and the series string power connections are always connected to the same two lines. Shifting of the current load from one line to the next is accomplished in the junction boxes.

This arrangement would allow all sections to be identical except for the tapered spacing in the array. A single 300 foot section may have from 2 to 6 transmitter modules and most of the 6 unit series strings will end in the center of section. This causes problems in stocking spare sections but this can be circumvented by the use of load resistors in the junction box which must be field alterable. For a further discussion on the field servicing problem, see Section II-e above.

The command line carries a pulsed single frequency tone which advances a counter in the clock module. The clock module, in turn, transmits a modified series of status bits as a recognition return to the receiver and modifies the number of double amplitude pulses on the clock line to command the transmitter modules.

The calibration signal uses a pseudo-random noise generator synchornized by the beginning of the noise test. (See Section VII below.)

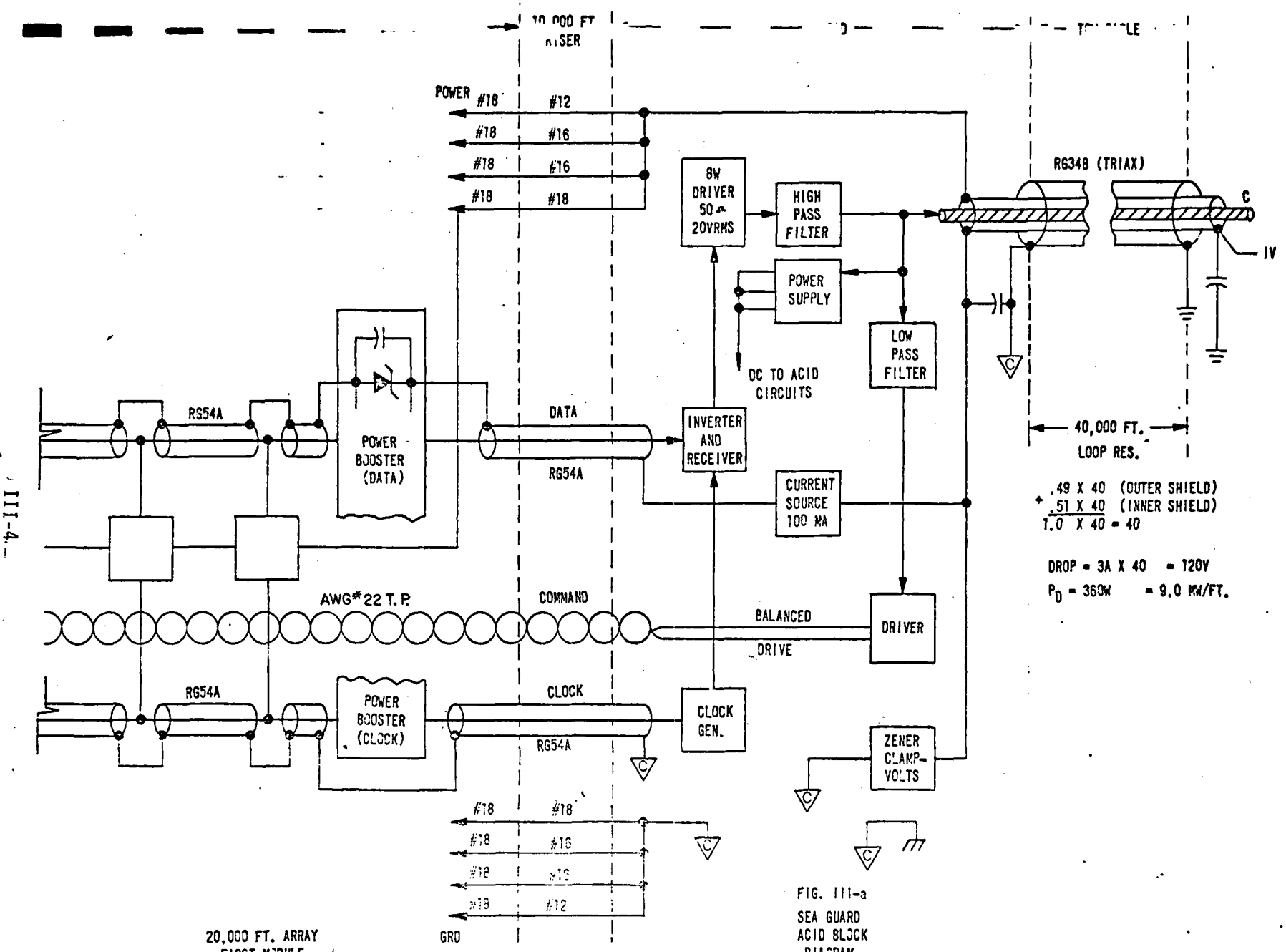
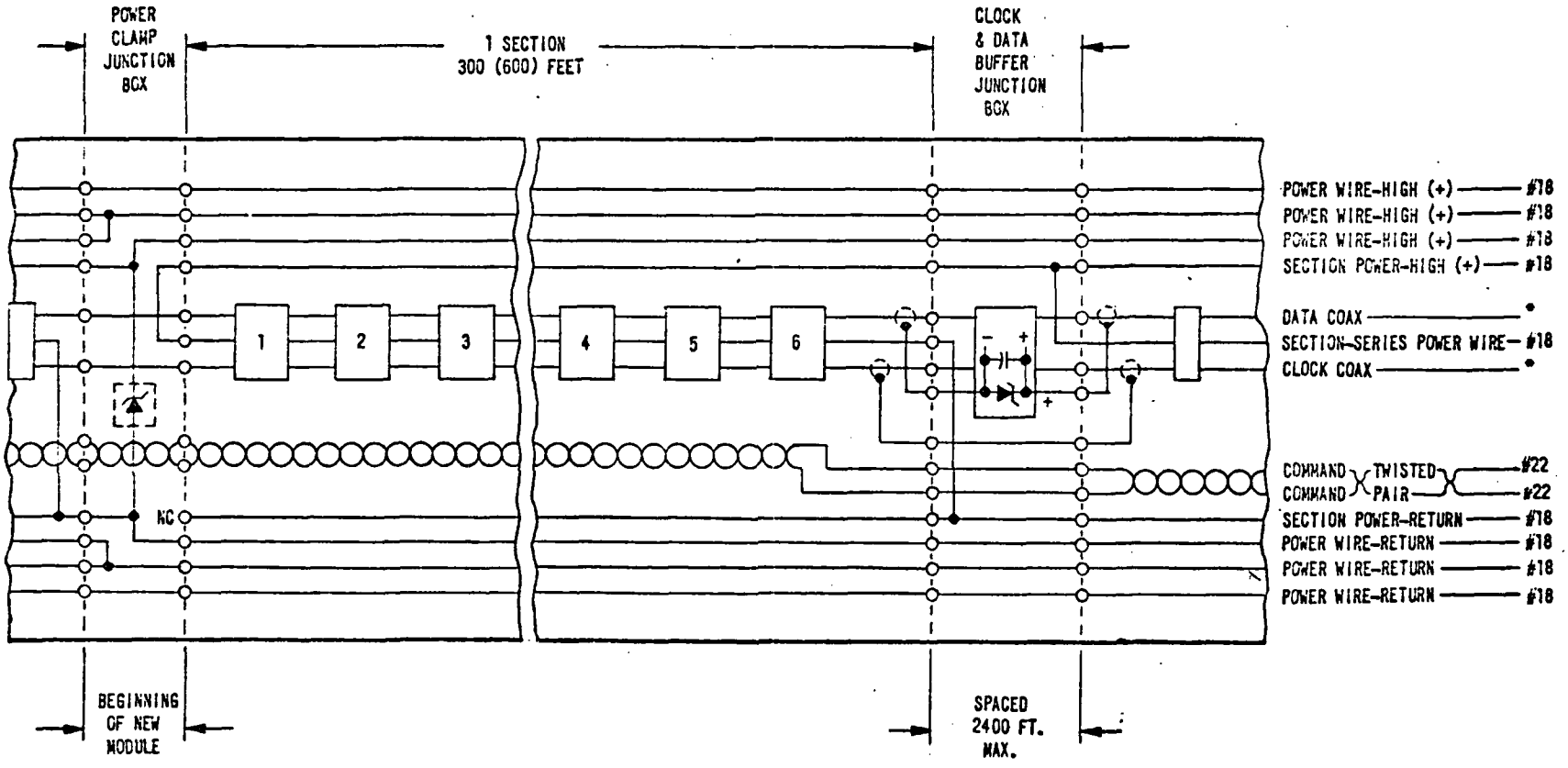


FIG. III-a
SEA GUARD
ACID BLOCK
DIAGRAM



NOTES:

1. ALL LINES CARRIED THROUGH JUNCTION BOX - TOTAL = (9) WIRES, (2) COAX, (1) TWISTED PAIR.
2. TOTAL CONNECTIONS = 15 INCLUDING SHIELDS.
3. DATA & CLOCK COAX SHIELDS CARRY 0.100 MA CURRENT TO POWER TO MAX.
   CLOCK & DATA BUFFERS - GND = CLOCK HIGH = DATA
4. * COAX LINES = .25" DIA MAX = RG54A.

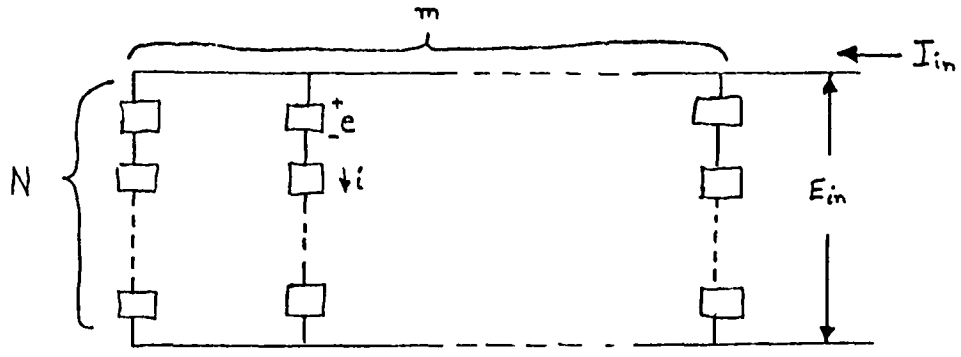
FIG. III-6

SEA GUARD
SECTION AND JUNCTION
DIAGRAM

IV. POWER DISTRIBUTION

2.1 TRADE-OFF STUDY

2.1.1 Series vs. Parallel Transmitter Connections



N = Number of transmitters in series

m = Number of parallel groups

i = Current per transmitter

e = Voltage across one transmitter

E_{in} = Ne

I_{in} = mi

Nm = 253

Limiting Cases:

All in series, N=1, m=253

E_{in} = 253e

I_{in} = i

All in parallel, N = 253, m = 1

$E_{in} = e$

$I_{in} = 253i$

For TLA power conditions:

$e = 16V$

$i = 0.050$ amp

All in series:

$E_{in} = 4048$ volts

$I_{in} = 0.050$ amp

All in parallel:

$E_{in} = 16$ volts

$I_{in} = 12.65$ amp

The limiting cases both offer severe problems. For all transmitters in series, the required voltage would be prohibitive from considerations of generating the voltage on the ship and from the problem of providing a high enough breakdown voltage on the cable insulation. For all transmitters in parallel, the high current would create very high voltage drops on the cables and would result in very high cable power dissipation. Obviously a compromise system of a series-parallel configuration is required.

Figure 1 shows the relationship between N, m, E_{in}, and I_{in} for different system configurations. For N = 5 and below the current, and hence line-drop, becomes the limiting factor. For N = 6 and greater, the required voltage is the limiting factor. A further requirement is that the voltage across the series string nearest the source cannot exceed 33N volts or one or more of the zener diodes in the transmitters will conduct. With this consideration in mind, another relationship can be generated between the configuration and the array power wire sizes. (Note: Based on latest TLA information this upper limit is 25.8 N volts.)

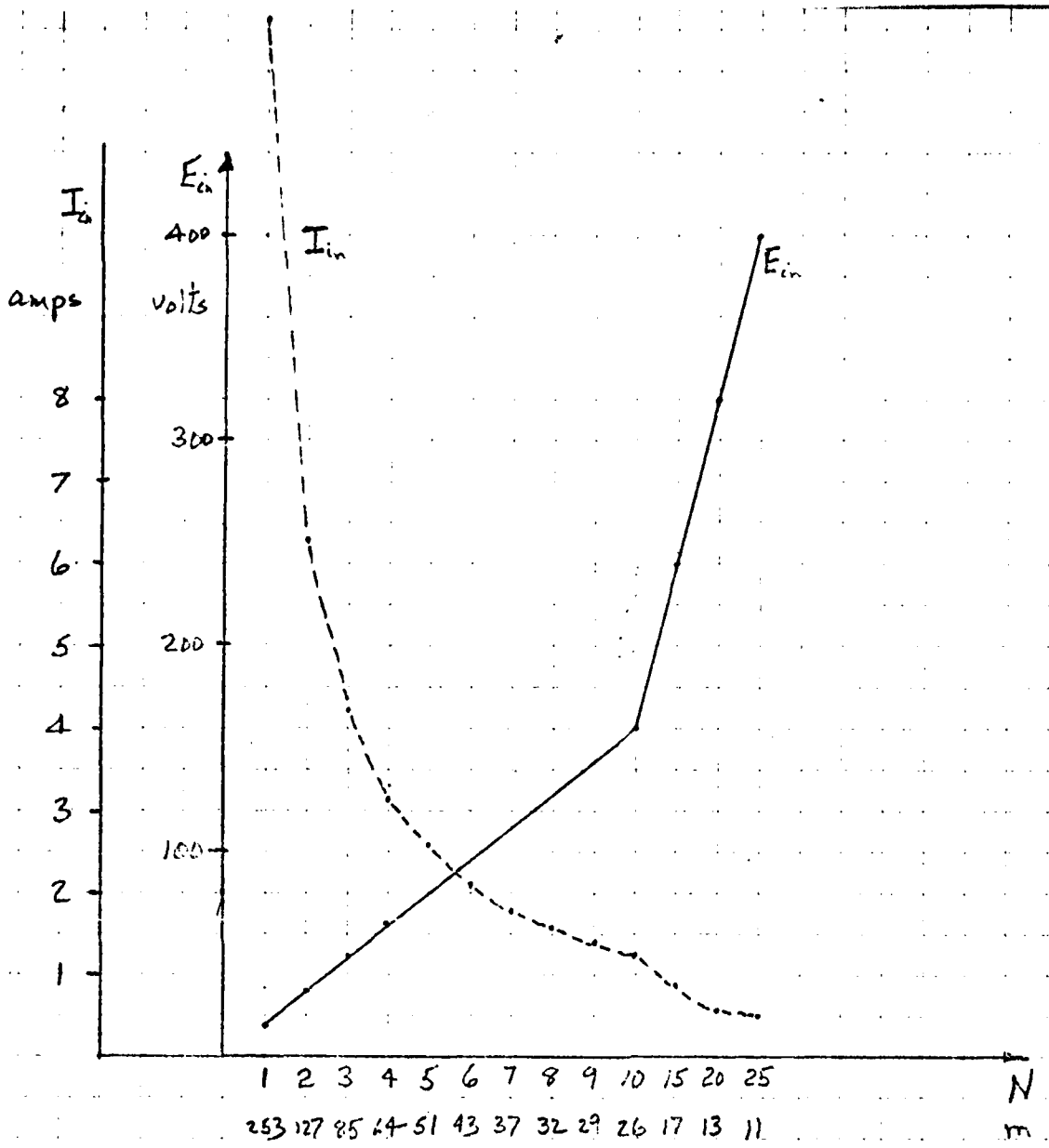

I_a
amps
E_{in}
volts
400
300
200
100
8
7
6
5
4
3
2
1
I_{in}
E_{in}
1 2 3 4 5 6 7 8 9 10 15 20 25
N
253 127 85 64 51 43 37 32 29 26 17 13 11
m

FIGURE 1

$$E_{min} = 16N$$

$$E_{source} = E_{min} + \frac{1}{2}(2L)\ I\ r_c$$

$$= E_{min} + .05\ mL\ r_c$$

$$33N > 16N + .05\ mLr_c$$

$$r_c < 340\ \frac{N}{mL}\ \text{ohms per 1000 feet}$$

For the arrays being considered the length, L, can vary from 3300 feet to 19,800 feet. The following tables show the relationship for N vs. wire size for the different configurations.

Configuration 1:

$$L = 3{,}300 \text{ feet}$$

$$m = \frac{63}{N}$$

$$r_c = 340\ \frac{N^2}{(63)(3.3)}$$

$$r_c = 1.635\ N^2$$

N	r_c Max	Wire Size Min	Two Conductor Wire Size Min
4	26.2	24	27
5	40.9	26	29
6	58.9	27	30
7	80.1	28	31
8	104.7	30	33
9	132.5	31	34

The results indicate that any reasonable size wire could be used in this configuration for handling power.

Configuration II:

L = 6600 feet

$m = \frac{63}{N}$

$r_c = 0.818\ N^2$

N	r_c Max	Wire Size Min	Two Conductor Wire Size Min
4	13.1	21	24
5	20.4	23	26
6	29.4	24	27
7	40.1	25	28
8	52.3	27	30
9	66.2	28	31

The results again indicate that any reasonable size wire could be used to distribute power in the array.

Configuration III:

L = 6600 feet

$m = \frac{126}{N}$

$r_c = 0.409\ N^2$

N	r_c Max.	Wire Size Min	Two Conductor Wire Size Min
4	6.54	18	21
5	10.22	20	23
6	14.72	21	24
7	20.03	22	25
8	26.17	24	27
9	33.12	25	28

The results indicate that any wire larger than AWG 18 can be used for any of the values of N.

Configuration IV:

$L = 13{,}200$ feet

$m = \frac{126}{N}$

$r_c = 0.204\ N^2$

N	r_c Max	Wire Size Min	Two Conductor Wire Size Min
4	3.27	15	18
5	5.11	17	20
6	7.36	18	21
7	10.02	19	22
8	13.08	21	24
9	16.56	22	25

The results above indicate that wire size is becoming more constraining as the array gets larger, however, the wire sizes are still reasonable.

Configuration V:

$L = 9{,}900$ feet

$m = \frac{126}{N}$

$r_c = 0.273\ N^2$

N	r_c Max	Wire Size Min	Two Conductor Wire Size Min
4	4.36	16	19
5	6.81	18	21
6	9.81	19	22
7	13.36	21	24
8	17.44	22	25
9	22.08	23	26

For the above configuration, the wire sizes are still reasonable.

Configuration VI:

$L = 19{,}800$ feet

$m = \frac{253}{N}$

$r_c = 0.068\ N^2$

N	r_c Max	Wire Size Min	Two Conductor Wire Size Min
4	1.086	10	13
5	1.697	12	15
6	2.443	13	16
7	3.326	15	18
8	4,344	16	19
9	5.498	17	20

With the complete array entirely wired in series (power-wise) the wire sizes are too large for consideration. A further analysis of wire size is made in section 2.1.4 to relate other configurations of power connections.

CONCLUSION:

The choice of the number or transmitters in series seems to be arbitrary between 6 and 9. However, in-order-to keep the highest voltages in the array less than 200 volts, it is suggested that 6 transmitters be connected in series. Since the TLA system is configured with 6 transmitters in series, additional data can be obtained on power distribution in that configuration.

2.1.2 Use of DC or DC/DC Converters

The only apparent advantage to the use of DC/DC converters is to enable

the transmission of power at high voltage and low current to reduce transmission line losses. However, the above discussion demonstrates that the trade-off of series/parallel transmitter combinations can be used for the same effect. It is therefore, suggested that no further considerations be given to the use and design of DC/DC converters.

Power conditioners might be used to reduce power line transmitted noise or to cause the system to fail soft in the event of a partial failure. The present TLA transmitter design includes these features. A zener diode is used to bypass a transmitter if the internal load is reduced. Another area of possible use of voltage limiting is in ACID to limit the maximum voltage delivered to the array in the event that a portion of the load is removed.

It is suggested that voltage limiting circuits be placed at the beginning of each array. The following table lists the voltage sensitivities for the suggested configurations in the event one string of six transmitters is opened from the power lines.

Array	Change in Array Input	
	Parallel Signal	Series Signal
1	6.4 V	6.4 V
2	6.7 V	8.2 V
3	7.9 V	10.3 V
4	8.0 V	8.0 V

2.1.3 Cable Power Dissipation

$$\text{Riser Cable} = I_1^2 R_{R1} + I_2^2 R_{R2} + I_3^2 R_{R3} + I_4^2 R_{R4}$$

$$\text{Array Through Wires} = \left(I_2^2 + I_3^2 + I_4^2\right)\left(R_{A1}\right) + I_3^2 R_{A2} + I_4^2 (R_{A2}/2) + I_4^2 (R_{A3}/2) + (.275)^2 (R_{A4}/3)$$

$$\text{Transmitters} = E_{AV1}(.05)m_1 + E_{AV2}(.05)\,m2 + E_{AV3}(.05)m_3 + E_{AV4}(.05)m_4$$

$$\text{Power in Array Wire} = I_1 V_1 + I_2 V_2 + I_3 V_3 + I_4 V_4$$

$$\text{Clock} = E_{CLOCK}(.1)$$

Where I_N = Current to array N

m_N = Number of 6 transmitters strings in Array N

V_N = Voltage across Array N

E_{AVN} = Average voltage across Array N

E_{CLOCK} = Voltage at end of Array with clock

Table 1 contains the data for the arrays as calculated by the above equations. Figures 2 and 3 show the relative distribution of the power.

If one lets the efficiency of the system be related as follows:

$$\text{eff.} = \frac{\text{Power In Transmitters}}{\text{Power In}} \times 100\%$$

Then Table 2 relates the efficiency for the system. This does not include losses in the ship-to-ACID cable. Configurations are as shown in Figures 5 and 6.

PARALLEL SIGNAL DISTRIBUTION

Array	Riser	Through Wires	Array Wire	Transmitters	Clock
1	54	96	10	77	11
2	18	24	5	69	13
3	11	9	5	62	12
4	13	2	3	65	12

SERIAL SIGNAL DISTRIBUTION

Array	Riser	Through Wires	Array Wire	Trans-mitters	Clock
1	39	78	6	77	--
2	20	19	3	70	--
3	20	9	3	60	--
4	13	2	3	65	12

TABLE 1. POWER DISTRIBUTION

POWER DISTRIBUTION

PARALLEL SIGNAL DISTRIBUTION

(CONFIGURATION OF FIGURE 5)

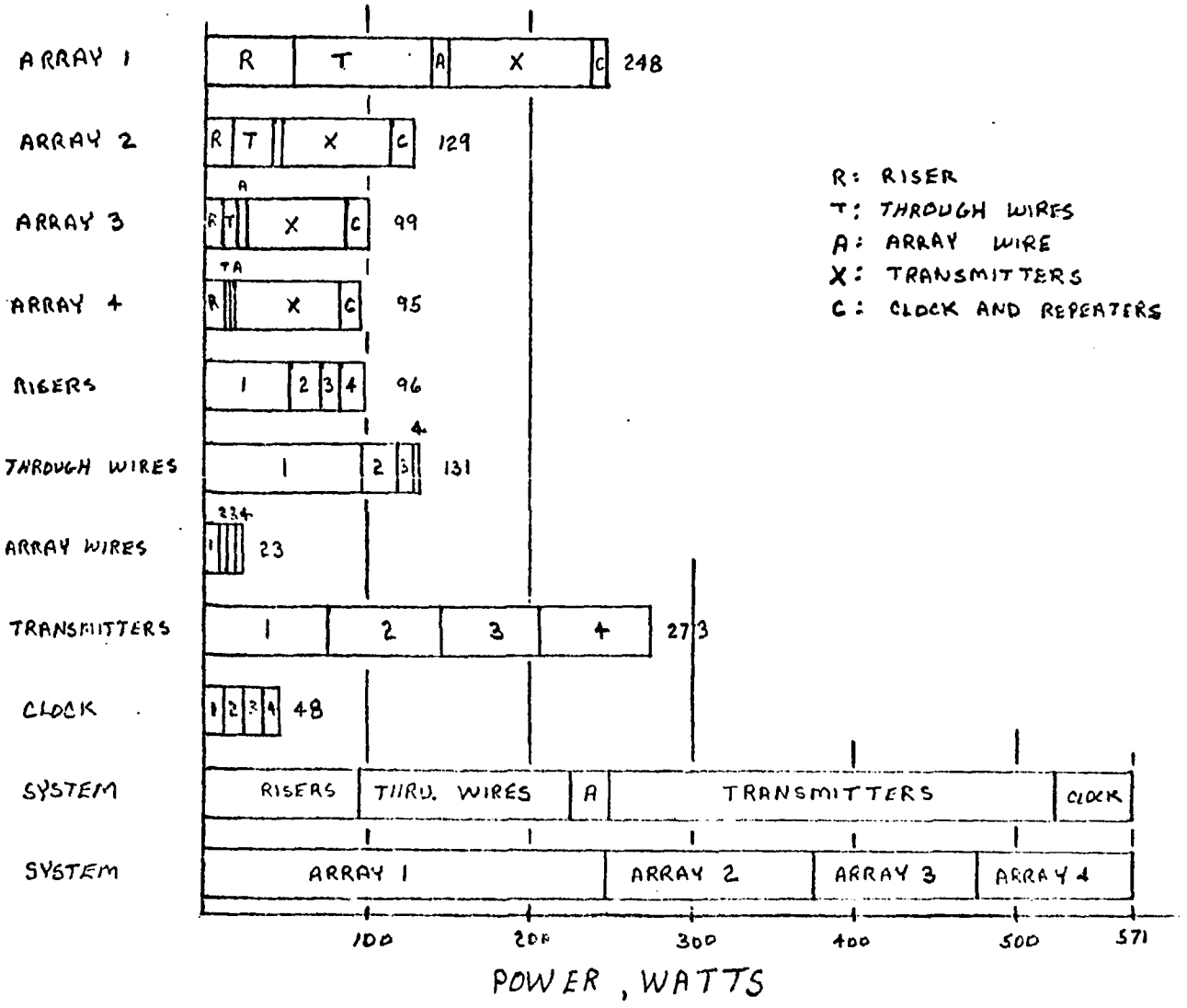


FIGURE 2

POWER DISTRIBUTION

SERIAL SIGNAL DISTRIBUTION

(CONFIGURATION OF FIGURE 6)

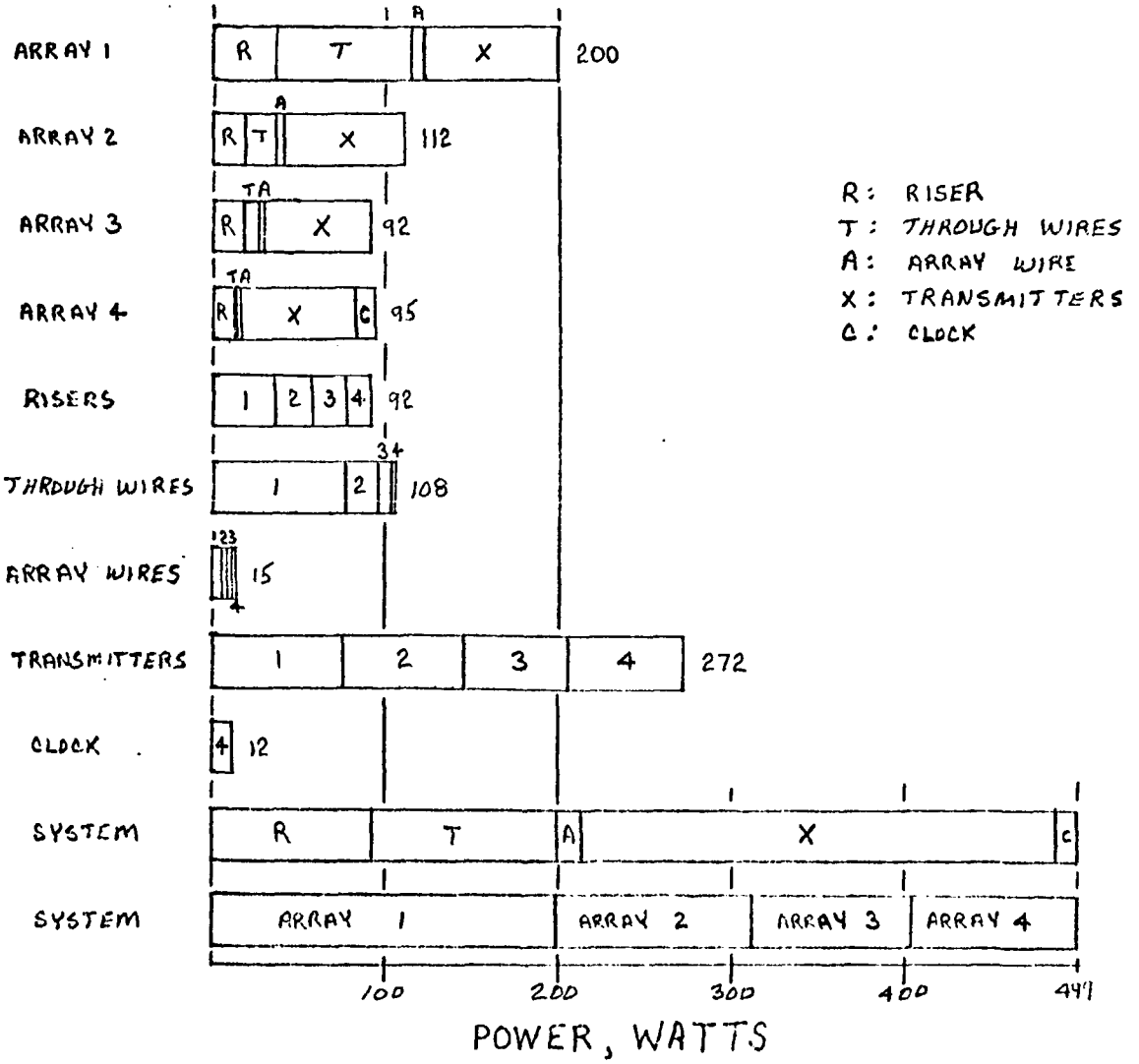


FIGURE 3

	EFFICIENCY	
	Parallel Signal Distribution	Serial Signal Distribution
Array 1	52%	61%
Array 2	50%	61%
Array 3	45%	53%
Array 4	44%	44%
System	48%	55%

TABLE 2

2.1.4 Cable Wire Size Requirements

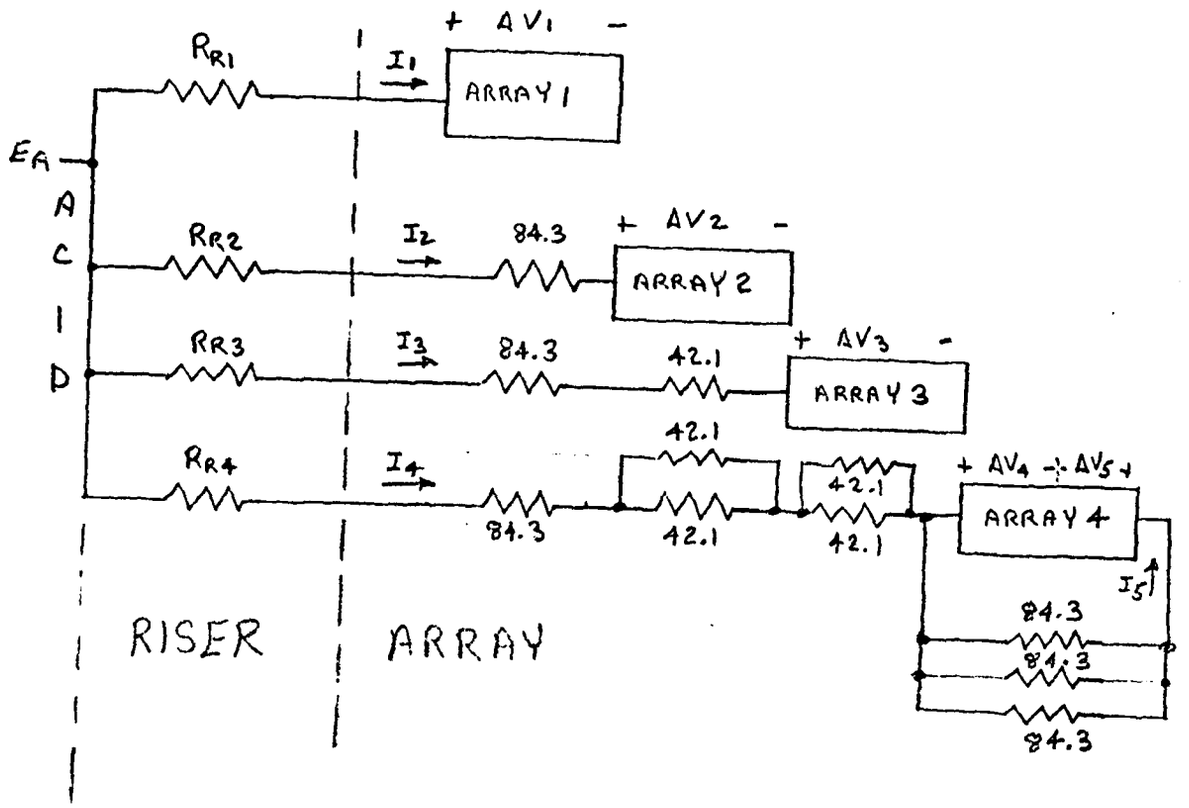
Selecting the wire sizes for the array is a complexed task involving the distributed loads of the transmitters. Several approaches were investigated before the final selection was made. Data on these preliminary investigations are included in Appendix A.

The following "ground rules" were used in the evaluation:

1. Let all arrays have four AWG 18 wires running through them.
2. Parallel power wires at array junction boxes to provide lower resistance paths as in Figure 5.
3. Select riser wire sizes to provide for array voltages within the limits of 113 and 165 volts for six transmitters connected in series.
4. Use the nonlinear taper of the transmitter spacing as described in the "Systems Constraints" with the densest spacing at the center of the overall array.

Figure 4 shows the system with lumped constant resistances representing the distributed wire resistances.

A further requirement that the riser and array wires be of the same sizes, is considered in Appendix B.



RESISTANCE THROUGH ARRAYS 1 & 4

$= 2 \cdot 6.385\ \Omega/1000\ FT \cdot 6.6\ 1000\ FT$

$= 84.3\ \Omega$

RESISTANCE THROUGH ARRAYS 2 & 3

$= 2 \cdot 6.385\ \Omega/1000\ FT \cdot 3.3\ 1000\ FT$

$= 42.1\ \Omega$

FIGURE 4

For the parallel signal distribution method the following data exist:

$$I_1 = 0.65 \text{ amp}$$

$$\Delta V_1 = 31.6 \text{ volts}$$

$$I_3 = I_2 = 0.6 \text{ amp}$$

$$\Delta V_3 = \Delta V_2 = 16.9 \text{ volts}$$

$$I_4 = 0.65 \text{ amp}$$

$$\Delta V_4 = 10 \text{ volts}$$

$$\Delta V_5 = 7.7 \text{ volts}$$

$$I_5 = 0.275 \text{ amp}$$

Because of the resistance in parallel with Array 4, the minimum voltage occurs inside the array.

If the minimum voltage allowed across a string of six transmitters is 113 volts, then the following conditions exist:

$$E_A = R_{R1}I_1 + 31.6 + 113 = R_{R1}I_1 + 144.6$$

$$E_A = R_{R2}I_2 + 16.9 + 50.6 + 113 = R_{R2}I_2 + 180.5$$

$$E_A = R_{R3}I_3 + 75.8 + 16.9 + 113 = R_{R3}I_3 + 205.7$$

$$E_A = R_{R4}I_4 + 83 + 10 + 113 = R_{R4}I_4 + 206$$

If $R_{RN} = 20\ r_{RN}$ then,

$$E_A = 13\ r_{R1} + 144.6$$

$$E_A = 12\ r_{R2} + 180.5$$

$$E_A = 12\ r_{R3} + 205.7$$

$$E_A = 13\ r_{R4} = 206$$

In order to keep the ACID voltage as low as possible, choose riser wire 4 as AWG 12 and,

$$r_{R4} = 1.588\ \Omega/1000\ \text{feet},\ R_{R4} = 31.6\Omega$$

$$E_A = 13(1.588) + 205.7 = 227\ \text{volts}$$

Let $E_A = 228$ volts,

$r_{R1} = 6.34$	use AWG 18	$R_{R1} = 127.7\Omega$
$r_{R2} = 3.875$	use AWG 14	$R_{R2} = 50.5\Omega$
$r_{R3} = 1.775$	use AWG 12	$R_{R3} = 31.76\Omega$

Placing these values in the equations and solving, the following array voltages are derived:

$$E_{ACID} = 228\ \text{volts}$$

$$E_{IN1} = 145\ \text{volts}$$

$$E_{CLOCK1} = 113\ \text{volts}$$

$$E_{IN2} = 147\ \text{volts}$$

$$E_{CLOCK2} = 130\ \text{volts}$$

$$E_{IN3} = 133\ \text{volts}$$

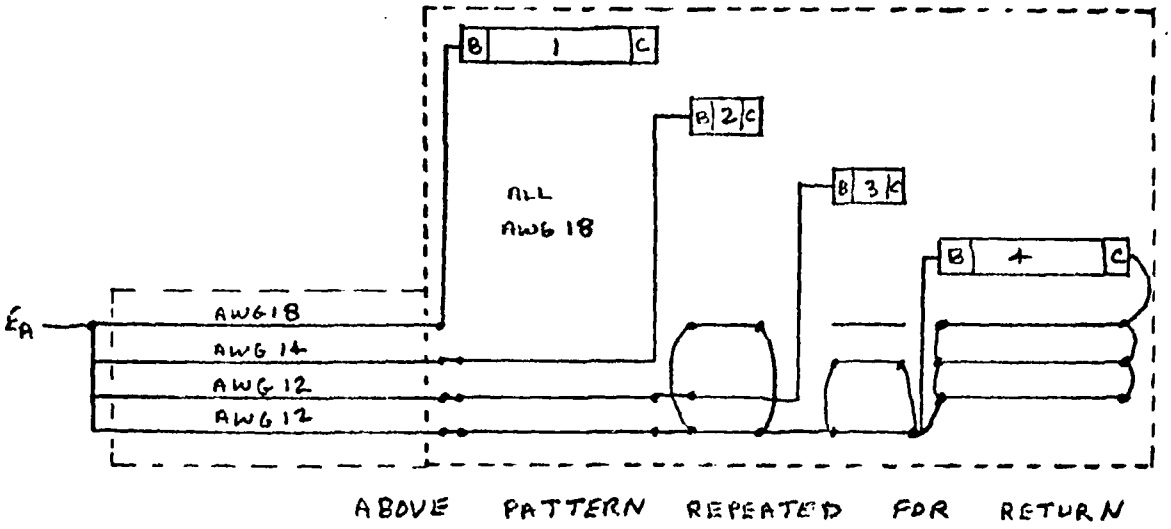
$$E_{CLOCK3} = 116\ \text{volts}$$

$$E_{IN4} = 124\ \text{volts}$$

$$E_{LOW4} = 114\ \text{volts}$$

$$E_{CLOCK4} = 117\ \text{volts}$$

These array voltages are all within the allowed range and are plotted in Figure 5.



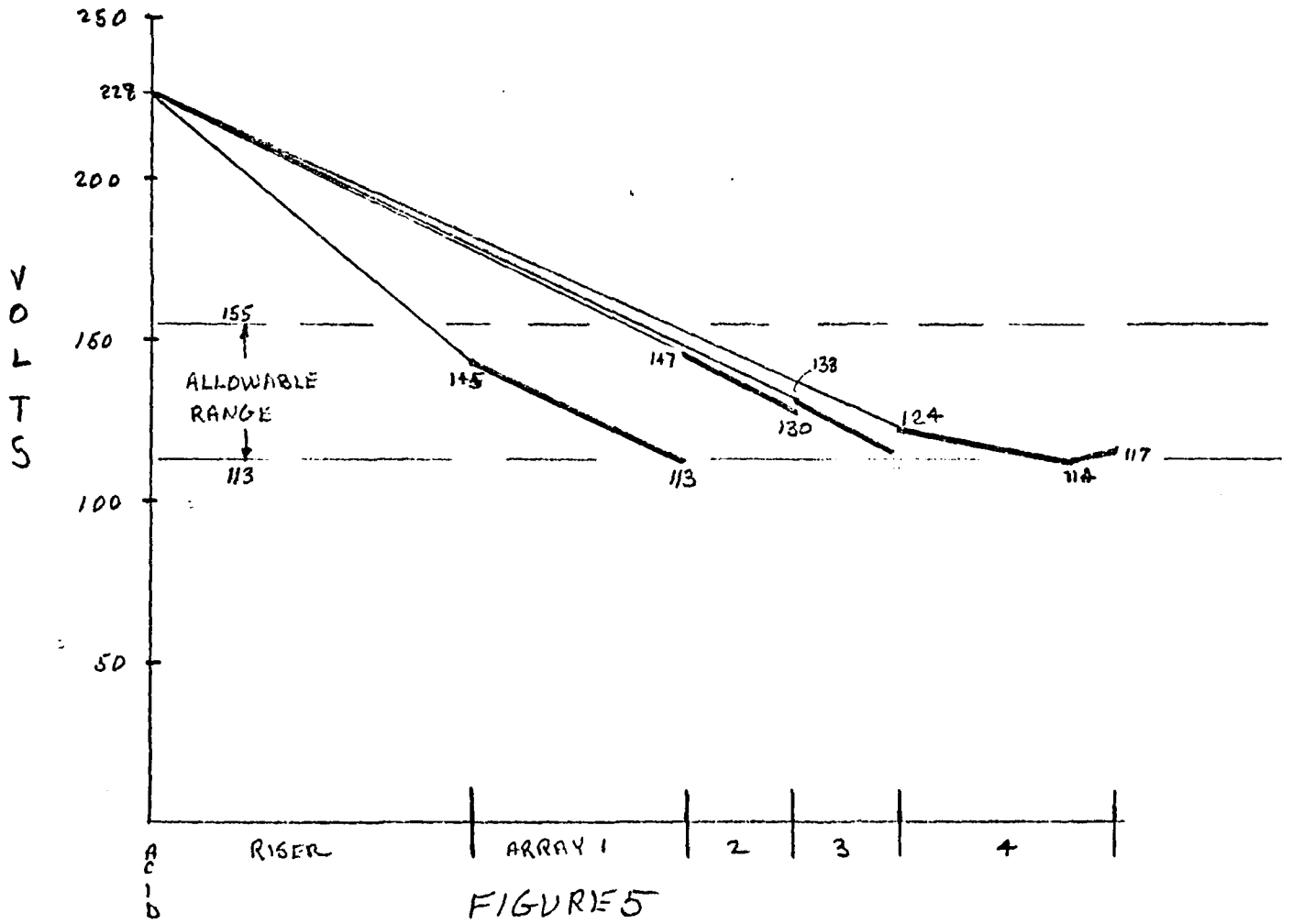


FIGURE 5

PARALLEL SIGNAL DISTRIBUTION

BUFFER AMPLIFIERS ON SEPARATE POWER

In a similar manner, given the following for a serial data distribution system,

I_1 = 0.55 amp

ΔV_1 = 23.2 volts

I_2 = 0.5 amps

ΔV_2 = 10.5 volts

I_3 = 0.5 amp

ΔV_3 = 10.5 volts

I_4 = 0.65 amp

ΔV_4 = 10 volts

ΔV_5 = 7.7 volts

I_5 = 0.275 amp

the following relationships exist:

$$E_A = 11\ r_{R1} + 136.2$$

$$E_A = 10\ r_{R2} + 165.65$$

$$E_A = 10\ r_{R3} + 186.7$$

$$E_A = 13\ r_{R4} + 206$$

Again, letting riser 4 equal AWG 12,

$E_A = 228$, $R_{R4} = 31.76\Omega$

$r_{R1} = 8.25$ use AWG 18 , $R_{R1} = 127.7\Omega$

$r_{R2} = 6.135$ use AWG 16 , $R_{R2} = 80.32\Omega$

$r_{R3} = 4.03$ use AWG 16 , $R_{R3} = 80.32\Omega$

this leads to the following data which are plotted in Figure 6.

E_{ACID} = 228 volts

$E_{IN}1$ = 145 volts

$E_{END}1$ = 113 volts

$E_{IN}2$ = 146 volts

$E_{END}2$ = 135 volts

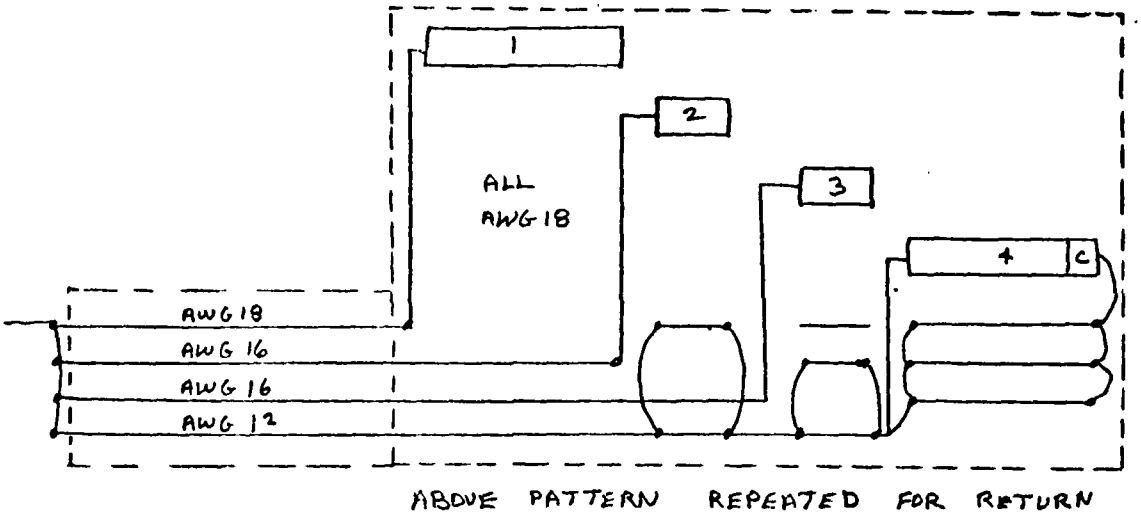
$E_{IN}3$ = 125 volts

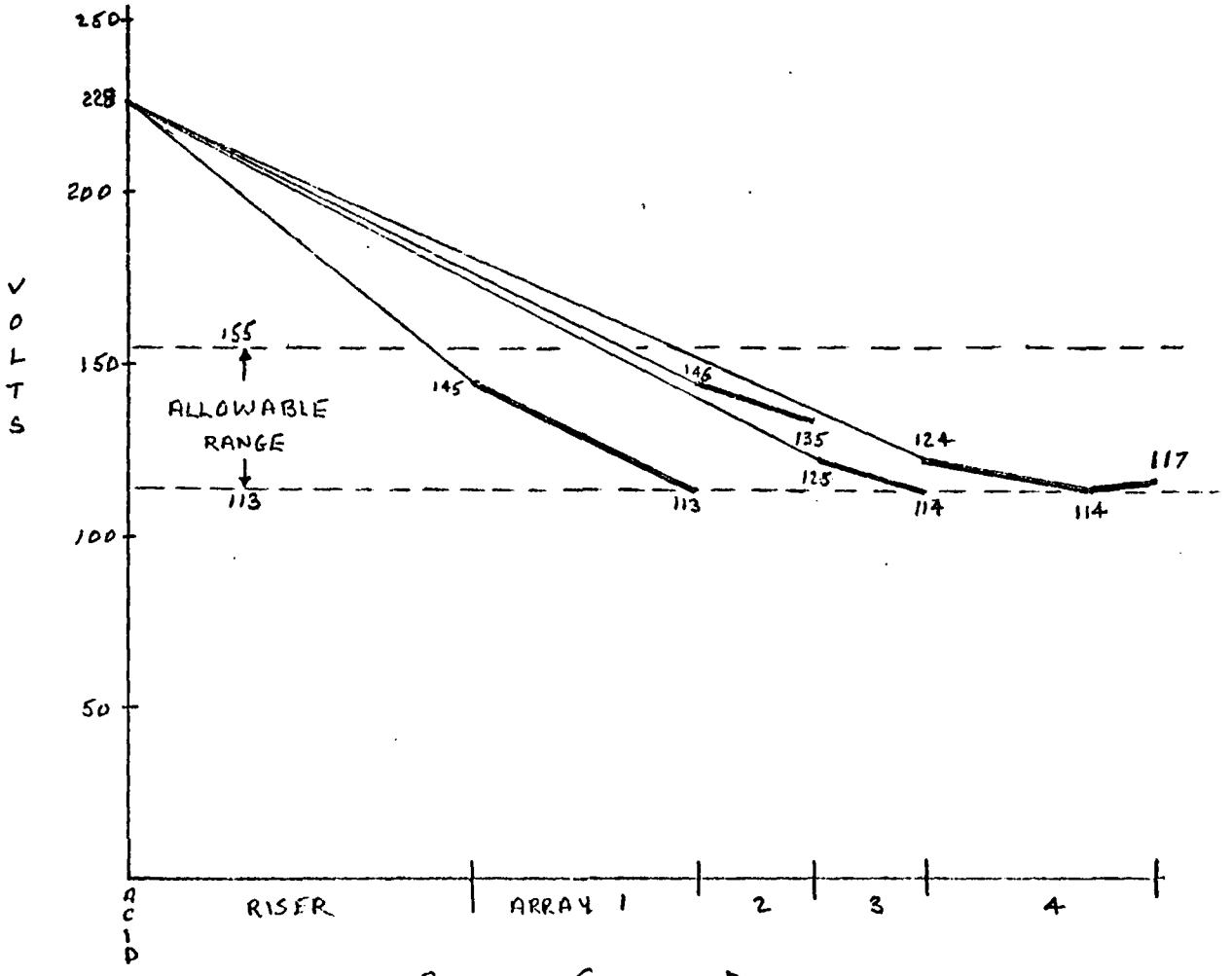
$E_{END}3$ = 114 volts

$E_{IN}4$ = 124 volts

$E_{LOW}4$ = 114 volts

E_{CLOCK} = 117 volts





SERIAL SIGNAL DISTRIBUTION

BUFFER AMPLIFIERS ON SEPARATE POWER

FIGURE 6

V. DATA TRANSMISSION SYSTEMS

6.0 DISCUSSION OF TRUNK AND ARRAY CABLE TRADE-OFFS

This section will evaluate the suitability of various types of cable for the transmission of the clock, data, and command signals through the Array, Riser, and Trunk cables of the Sea Guard System.

6.1 The types of cable considered for these functions are twisted pair, quad, coax, and triax. However, not all types are considered for all functions, due to ground-rule system constraints and the results of other trade-offs as follows:

(1) Only coax and triax (which is in fact coaxial) are considered for the trunk application, due to the system constraint of one coaxial cable assumed for the trunk.

(2) Triax cables are not considered for any function in the riser or array cables, as the outer shields become unnecessary in view of the optimum power distribution system.

(3) The use of a quad for the command line in the riser and array is dismissed as uneconomical, since the optimum command format requires only two conductors.

(4) The evaluation of quads for use as data and clock lines has been set aside because of the attendant need to modify the input and output circuits of all telemetry modules for balanced operation. These cables exhibit poor and unpredictable cross-talk isolation between pairs when used with unbalanced sources or loads, especially at frequencies above 100 kHz.

The above exclusions leave only the trade-off decisions listed in Table 6.1. The decisions for the array and riser cables, however, must be considered for both single and multiple data systems in both the "hose" and "cable" configurations.

	Array Cable	Riser Cable	Trunk Cable
Clock	Pair vs. Coax	Pair vs. Quad vs. Coax.	Triax vs. Coax
Data	Pair vs. Coax	Pair vs. Quad vs. Coax	
Command	Pair vs. Coax	Pair vs. Coax	

TABLE 6.1 Cable Trade-Off Decisions

In paragraphs 6.1.1 through 6.1.4 below, the general characteristics and limitations of the various cables are discussed.

6.1.1 Twisted Pair

Two types of twisted pair are considered for Sea Guard transmission line applications. For the high frequency clock and data signals, shielded pairs are necessary to maintain predictably low levels of cross talk, especially with unbalanced sources and loads. For audio frequency command signals, however, unshielded pairs may well be the best choice especially since balanced operation will not require modification of existing hardware. Typical attenuation versus frequency curves are given for representative pairs in Figures 6-1 and 6-2.

6.1.2 Quads

See Paragraph 6.1.(4).

6.1.3 Coax

Coax cable with solid polyethylene dielectric material is considered for use in data and clock transmission, taking a variety of RG...U sizes to evaluate performance. Their attenuation curves are shown in Figure 6-3. These cables fall into six classes which are distinguished by their attenuation slopes and by the outer diameter of the polyethylene dielectric. Though

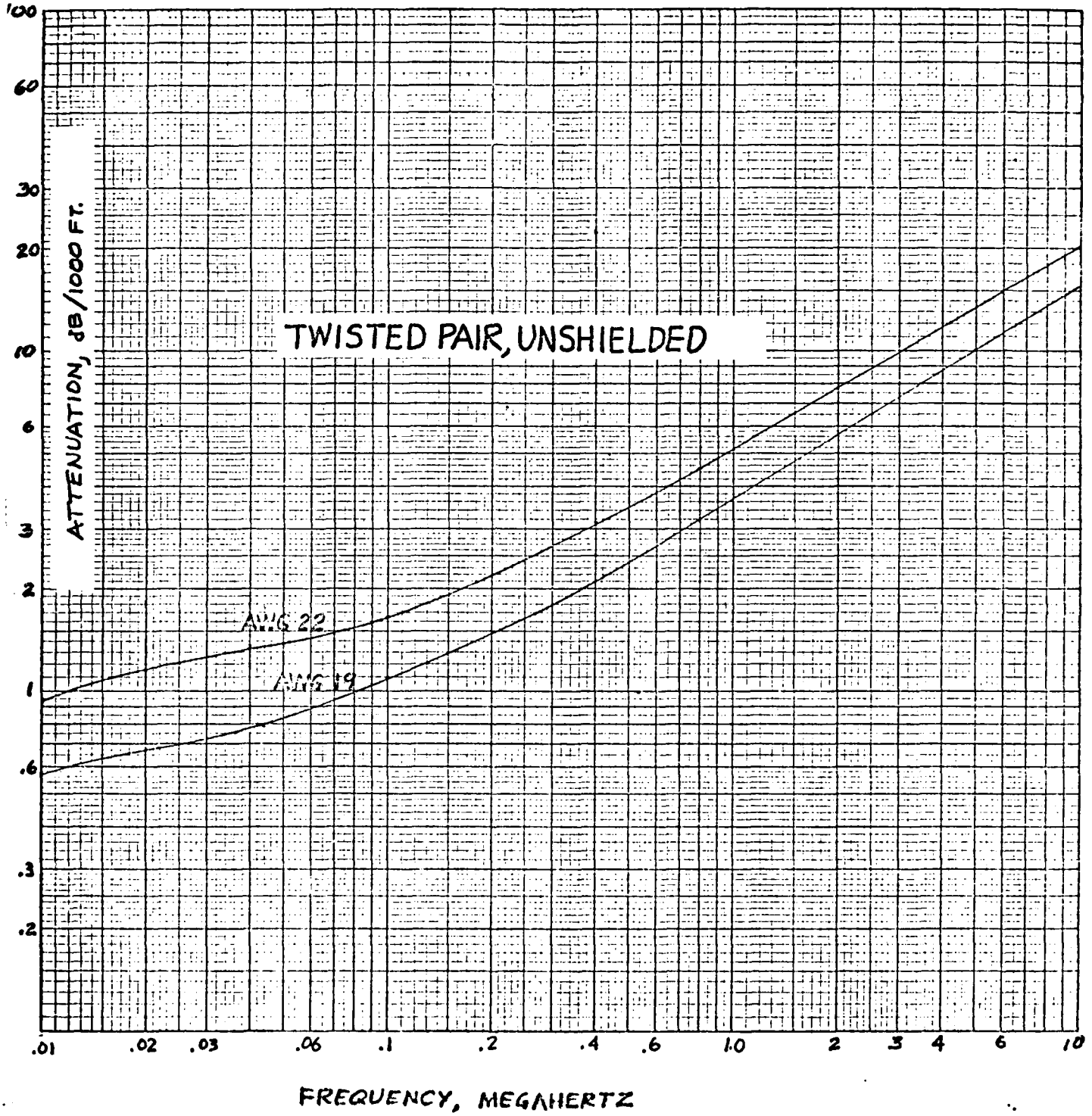
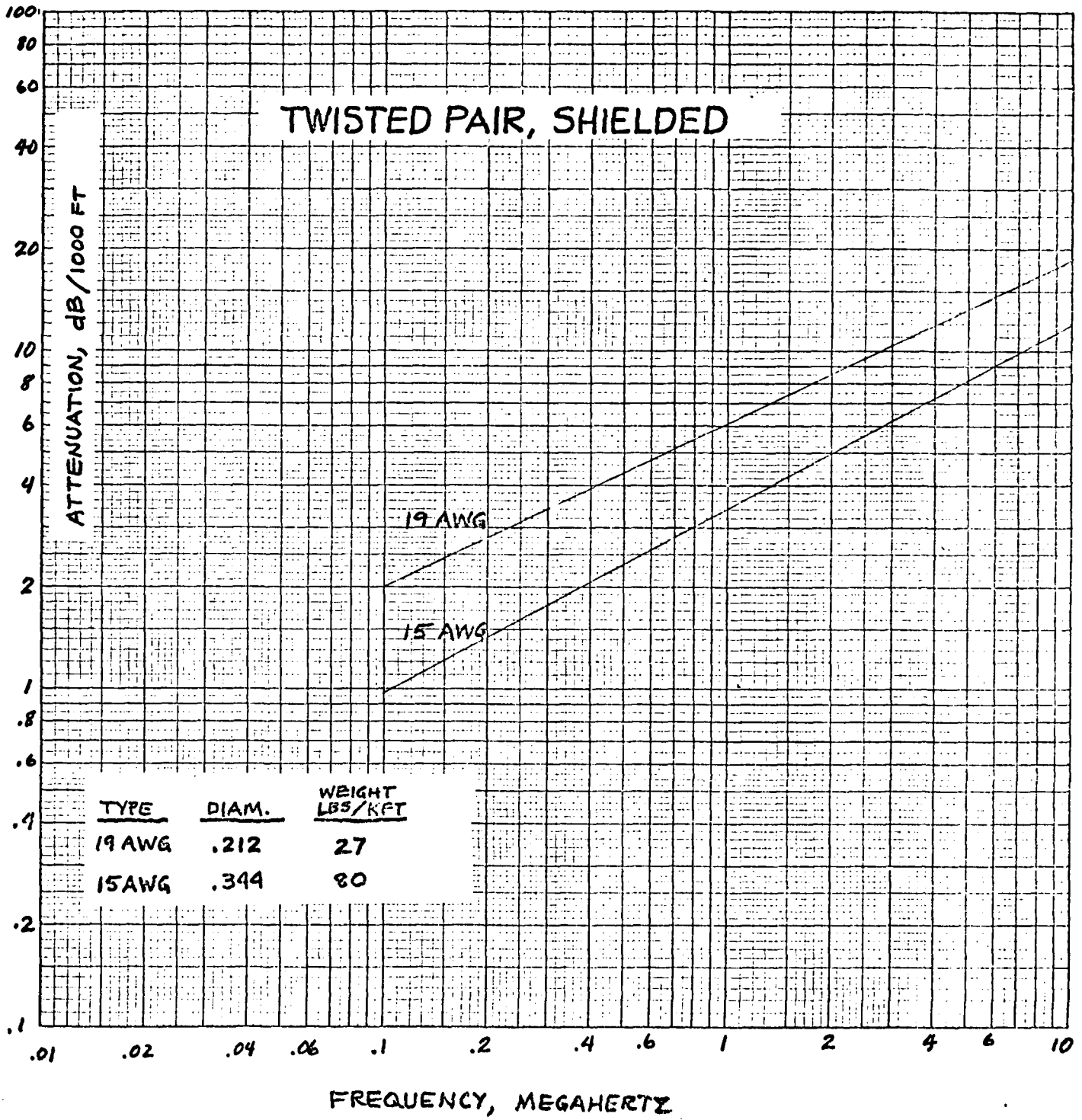

TWISTED PAIR, UNSHIELDED
ATTENUATION, dB/1000 FT.
100
60
30
20
10
6
3
2
1
.6
.3
.2
AWG 22
AWG 19
.01
.02
.03
.06
.1
.2
.4
.6
1.0
2
3
4
6
10
FREQUENCY, MEGAHERTZ

FIG. 6-1



TYPE	DIAM.	WEIGHT LBS/KFT
19 AWG	.212	27
15AWG	.349	80

339-1206 KEUFFEL & ESSER CO.
arith K 3 C

FIG. 6-2

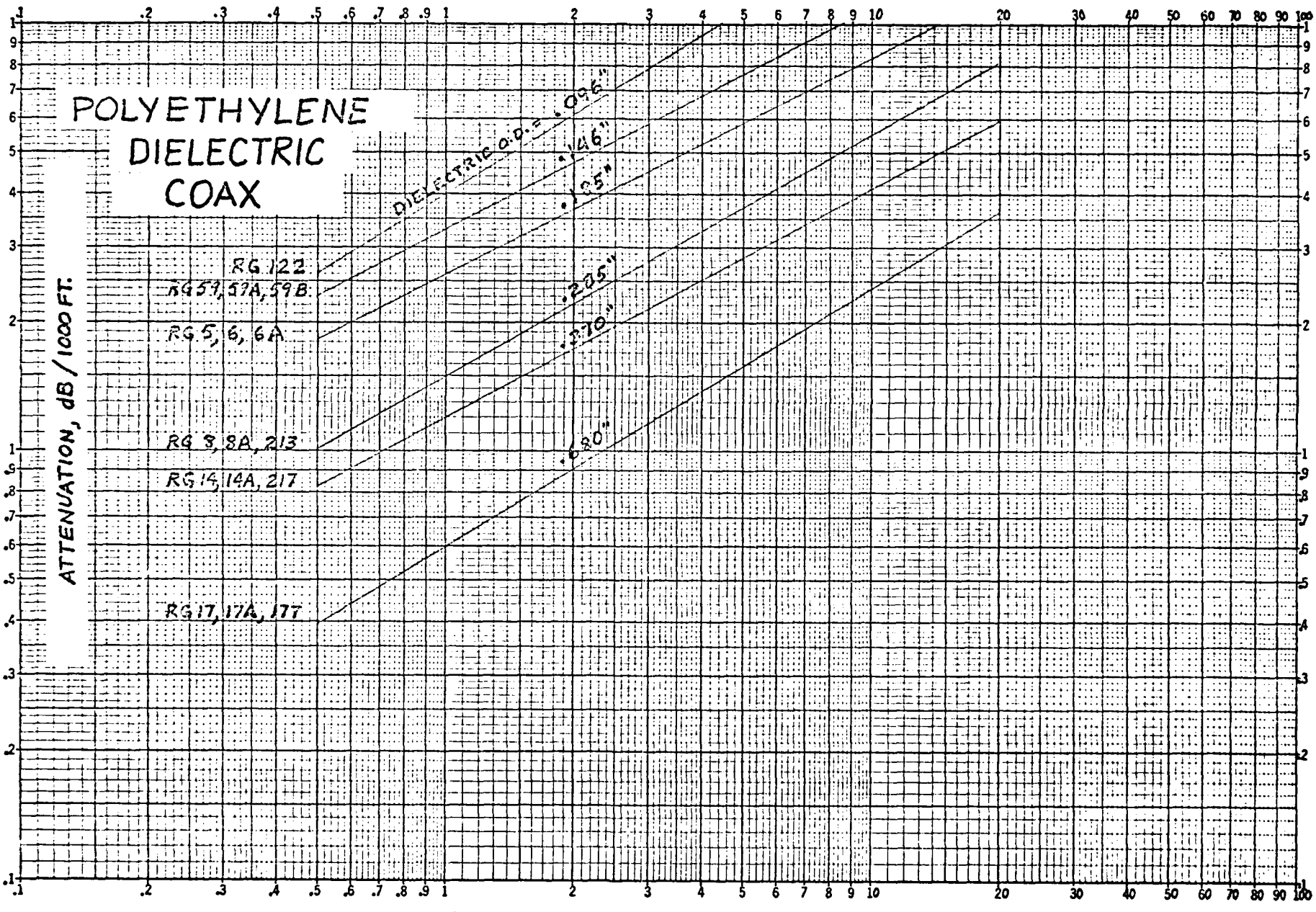

KE (RIT) '323
2 X 3 CYCLES MADE IN U.S.A.
KEUFFEL & ESSER CO.
POLYETHYLENE
DIELECTRIC
COAX
ATTENUATION, dB / 1000 FT.
FREQUENCY, MEGAHERTZ
DIELECTRIC O.D.=
.096"
.146"
.185"
.205"
.270"
.280"
RG 122
RG 59, 59A, 59B
RG 5, 6, 6A
RG 8, 8A, 213
RG 14, 14A, 217
RG 17, 17A, 177

FIG 6-3

the jacket diameters within a class may vary depending on number of braids, jacket thickness, and armor, the dielectric O.D. serves as a common denominator for classifying these coaxial cables with respect to attenuation. This is illustrated in Figure 6-4, where attenuation is plotted versus dielectric O.D. for six frequencies. Note that the data points conform quite well to linear slopes on the log x log plot. This forms a basis for projecting the values of attenuation at any of the six frequencies for a polyethylene coax with any desired value of dielectric O.D. between .15 and .70 inch.

Another dielectric material, tape-wound teflon, has a special potential for application in the trunk cable. For cables with a dielectric O.D. greater than .25 inch, the attenuation of the taped teflon cables is considerably less than for polyethylene or solid teflon. Attenuation versus dielectric O.D. is plotted for four such cables in Figure 6-5, with the corresponding polyethylene curves dotted in to show the slope difference and "break-even"point at about .25 O.D. (Some concern arises that the superior performance may be due to air space in the taped dielectric. However, Times Wire and Cable Corporation has expressed confidence that this is not the case, and that this dielectric is consistent with the 10,000 psi requirement. Rather, they say the low loss is due to a type of teflon which has a lower dissipation factor, but which cannot be conventionally extruded.)

The relationship between dielectric outer diameter and over-all jacket diameter for typical single-braid coax cables is shown in Figure 6-6.

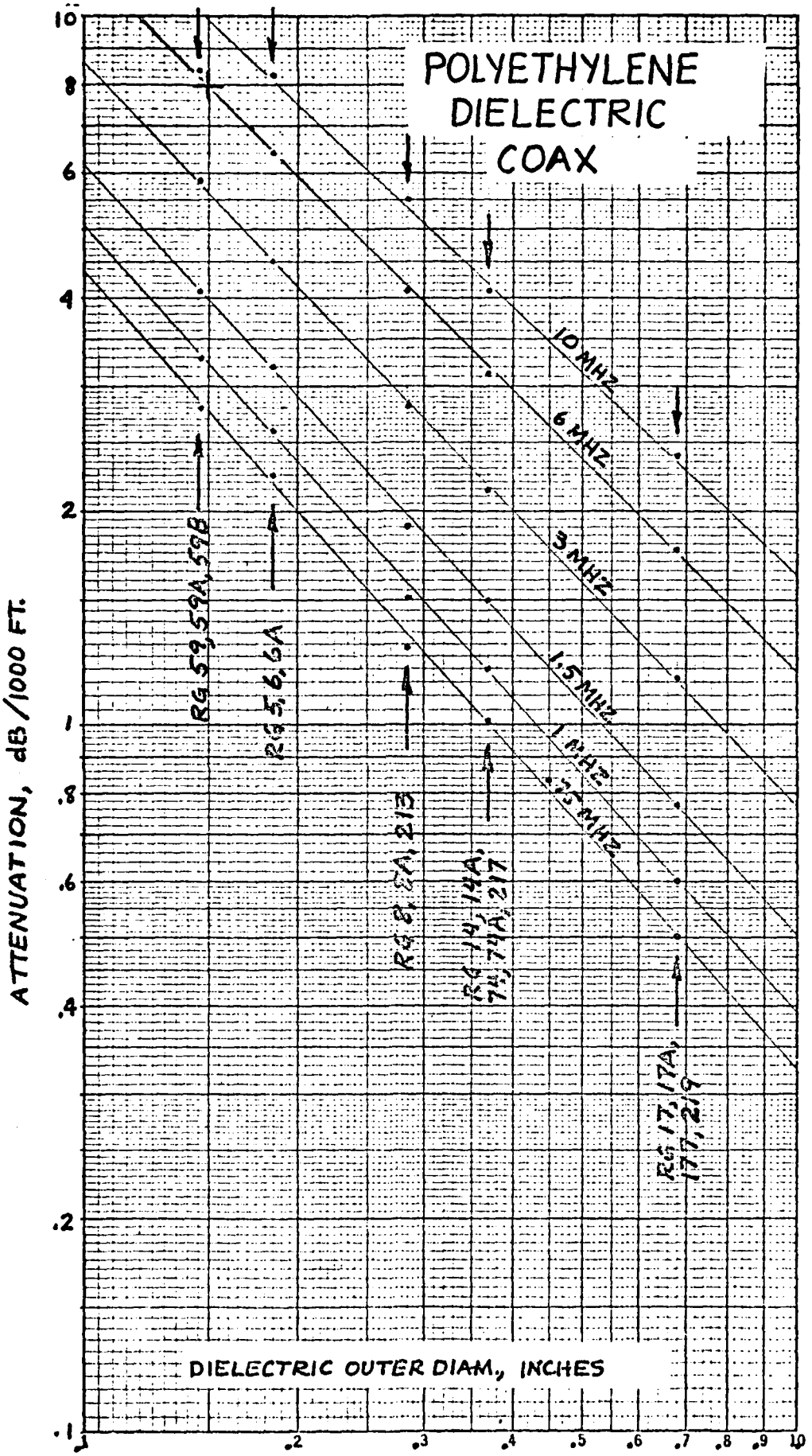

POLYETHYLENE
DIELECTRIC
COAX
ATTENUATION, dB/1000 FT.
DIELECTRIC OUTER DIAM., INCHES
10 MHZ
6 MHZ
3 MHZ
1.5 MHZ
1 MHZ
.5 MHZ
RG 59, 59A, 59B
RG 5, 6, 6A
RG 8, 8A, 213
RG 14, 14A, 74, 74A, 217
RG 17, 17A, 17D, 218
10
8
6
4
2
1
.8
.6
.4
.2
.1
.2
.3
.4
.5
.6
.7
.8
.9
1.0

FIG. 6-4

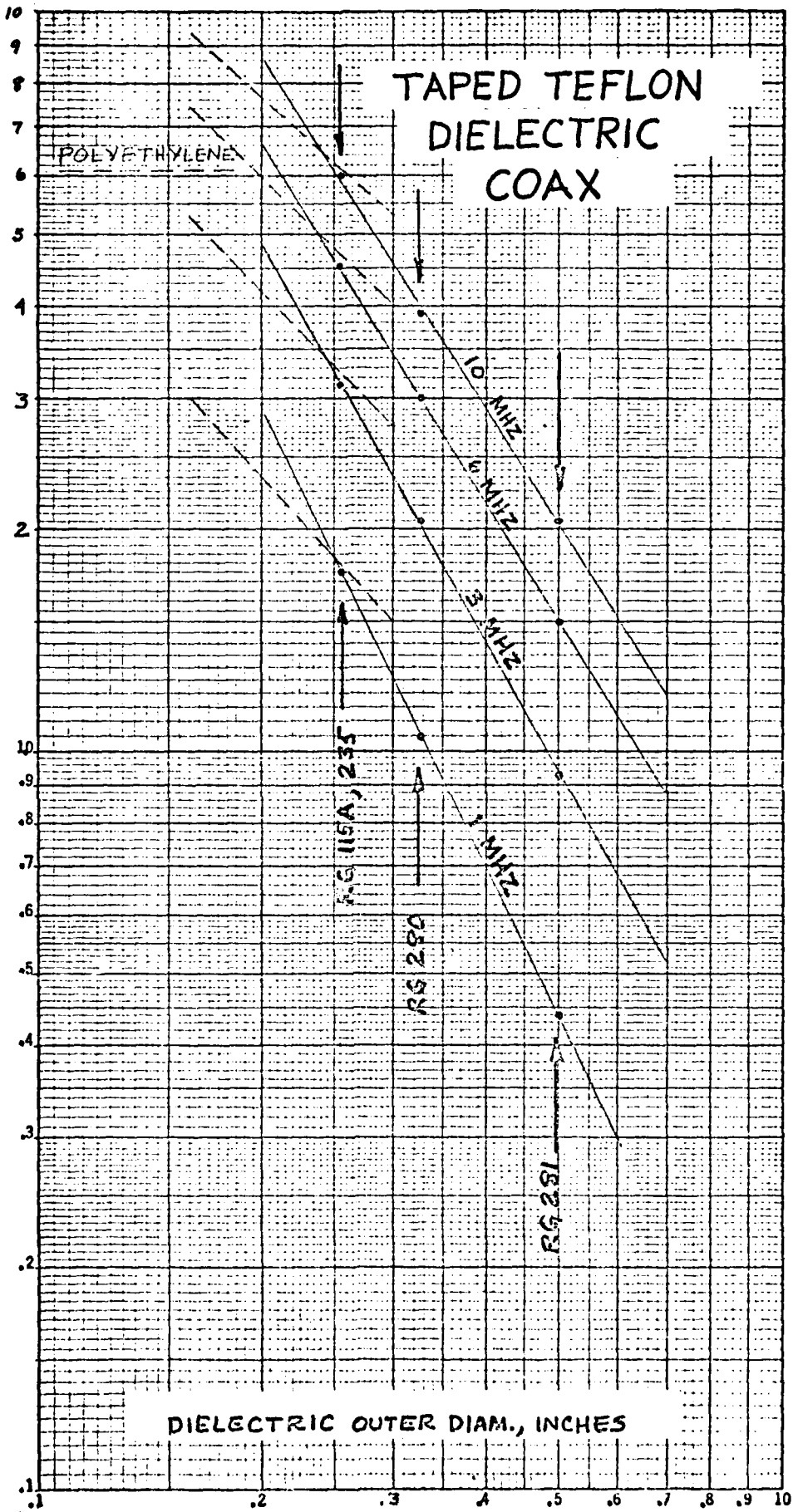

TAPED TEFLON DIELECTRIC COAX
POLYETHYLENE
10 MHZ
6 MHZ
3 MHZ
1 MHZ
RG 58A, 235
RG 290
RG 281
ATTENUATION, dB/1000 FT.
DIELECTRIC OUTER DIAM., INCHES
10
9
8
7
6
5
4
3
2
1
.9
.8
.7
.6
.5
.4
.3
.2
.1
.2
.3
.4
.5
.6
.7
.8
.9
10

FIG. 6-5

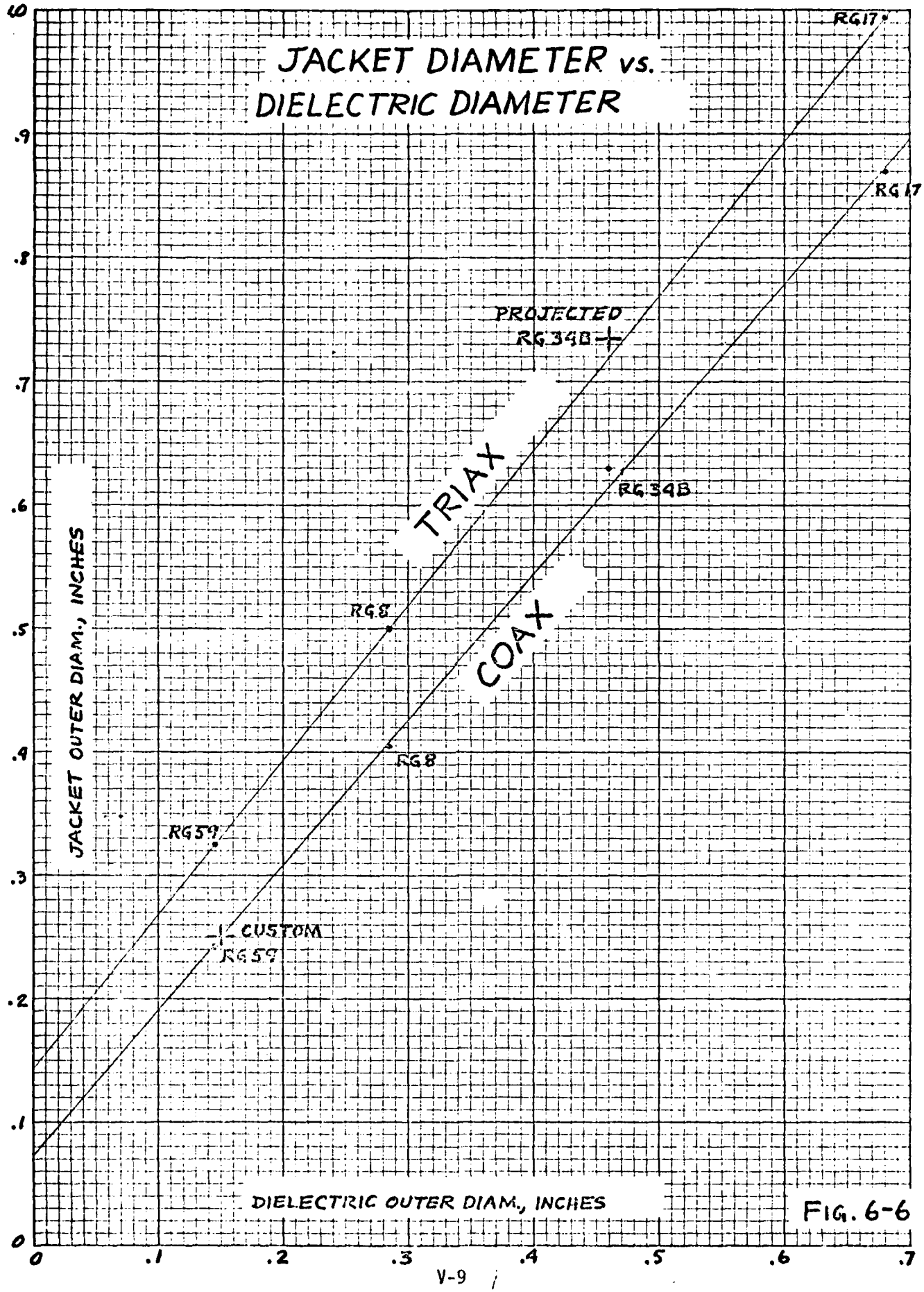

JACKET DIAMETER vs.
DIELECTRIC DIAMETER
JACKET OUTER DIAM., INCHES
DIELECTRIC OUTER DIAM., INCHES
RG17
RG 17
PROJECTED
RG 34B
RG34B
TRIAX
COAX
RG8
RG 8
RG59
CUSTOM
RG59
0
.1
.2
.3
.4
.5
.6
.7
.8
.9
.0

FIG. 6-6

6.1.4 Triax

Many types of RG...U coax cable are also available in triax configuration, which is achieved by the addition of a second shield separated from the first by a thin dielectric interlayer. Those types not already available in triax can readily be adapted from existing coax types. The electrical properties of the triax are unchanged, except for a substantial improvement in the EMI leakage. (An improvement of 40 dB for frequencies up to 1000 megahertz is typical.) The differences in diameter and weight between coax and the corresponding triax are shown in Figures 6-6, 6-7 and 6-8.

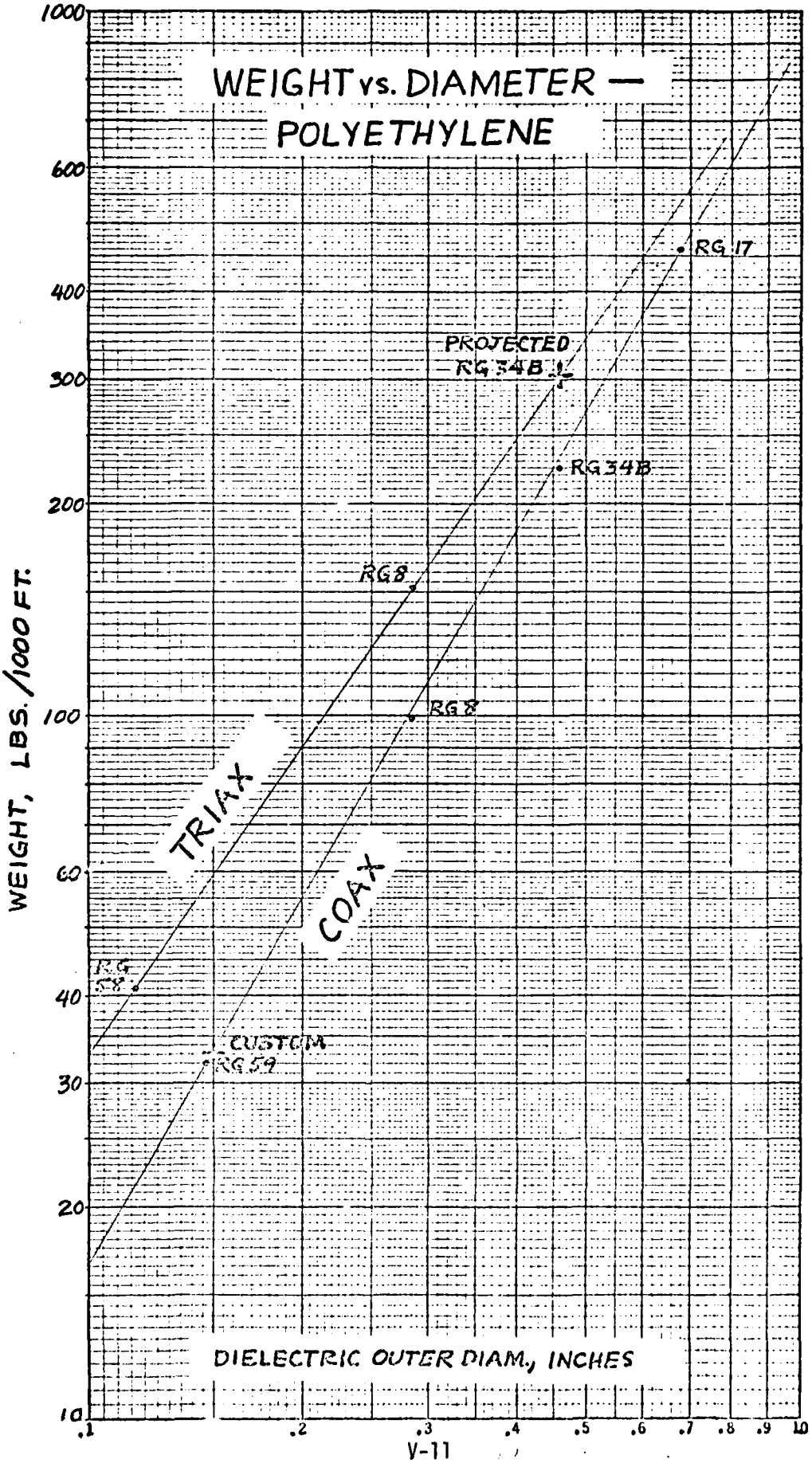

WEIGHT vs. DIAMETER —
POLYETHYLENE
WEIGHT, LBS./1000 FT.
1000
600
400
300
200
100
60
40
30
20
10
RG 17
PROJECTED
RG 34B
RG 34B
RG8
RG 8
TRIAX
COAX
RG 58
CUSTOM
RG 59
.1
.2
.3
.4
.5
.6
.7
.8
.9
1.0
DIELECTRIC OUTER DIAM., INCHES

FIG. 6-7

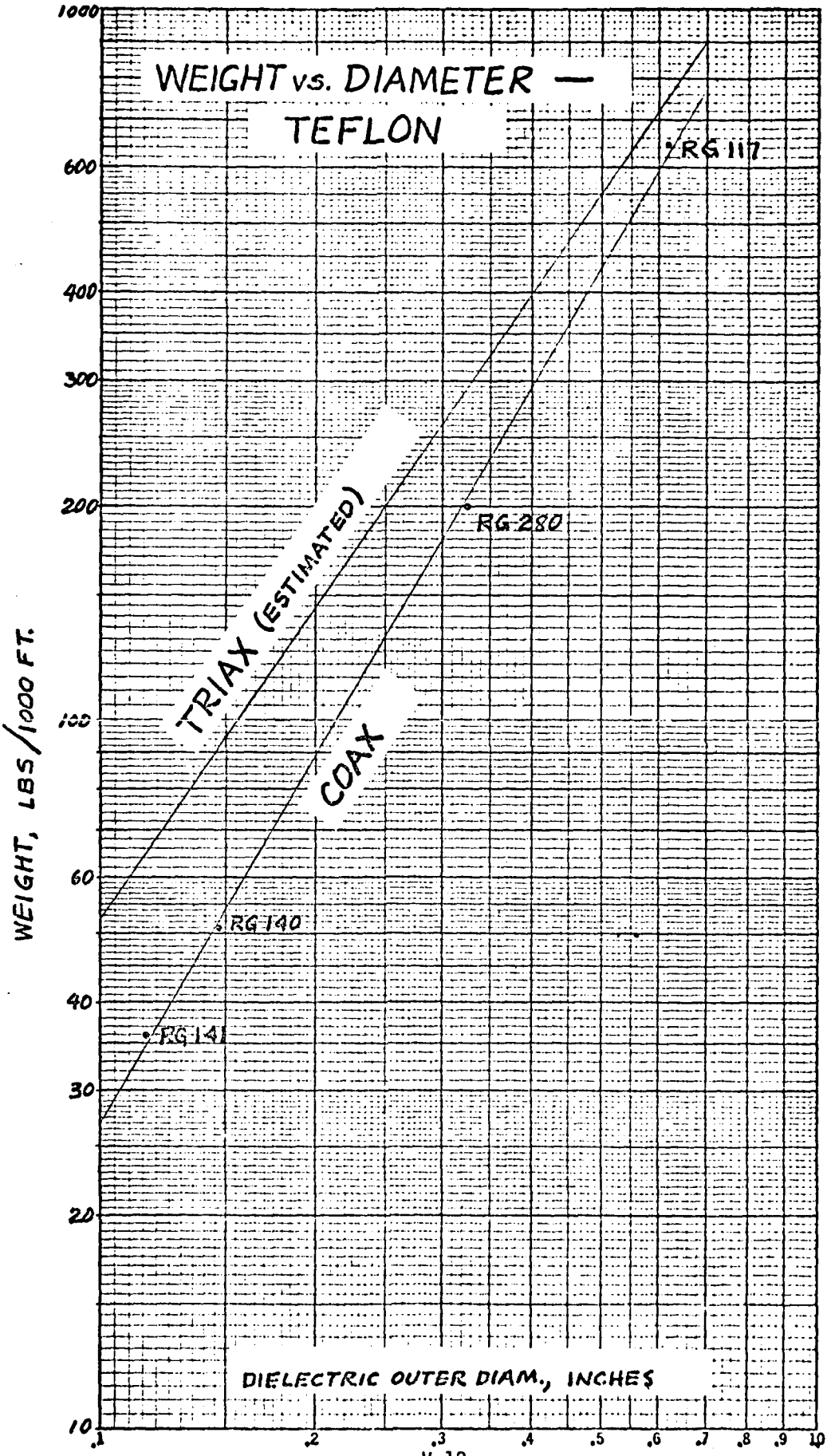

WEIGHT vs. DIAMETER —
TEFLON
RG 117
RG 280
TRIAX (ESTIMATED)
COAX
RG 140
RG 141
WEIGHT, LBS/1000 FT.
DIELECTRIC OUTER DIAM., INCHES
1000
600
400
300
200
100
60
40
30
20
10
.1
.2
.3
.4
.5
.6
.7
.8
.9
1.0

FIG. 6-8

6.2 This section will discuss the factors affecting specific trade-off decisions in selecting cables for the various functions. The simplest of the trade-offs to describe are those regarding the trunk cable and the command link in the riser and array, since these decisions are unaffected by configuration factors such as single versus multiple data channels and "hose" versus "cable" array mechanization. Therefore, these two trade-offs are presented below:

(a) Trunk Cable

Satisfying the trunk cable requirement within the 3/4 inch diameter constraint is made possible by eliminating the need for 6 MHz clock transmission to the surface. This is done by synthesizing a clock signal at the surface using the 3 mHz data stream as a phase reference. The 3 mHz attenuation allowance in the trunk is governed by the attainable practical data source level of 20 V peak at the ACID and a detection level of 2 millivolts peak considering the surface noise environment. The resulting 80 dB trunk loss allowance must be diminished by 9.54 dB to allow for failure of 2/3 of a triple redundant source, leaving 70.46 dB loss at 3 mHz allowed in the trunk cable. This represents a cable attenuation of 1.76 dB/KFT, which can be realized in a standard coax cable such as RG 34B, which has 1.54 dB/KFT attenuation at 3 mHz, for a total of 61.6 dB in 40,000 feet. A triax version of RG 34B, as projected from the diameter and weight curves of Figures 6-6 and 6-7 is compared below to the RG 34B coax, which has a .460" dielectric O.D.

	Total 3 mHz Attenuation	Jacket Diameter	40 KFT Weight
RG 34B coax	61.6 dB	.630"	8,960 lbs.
RG 34B triax	61.6 dB	.735"	12,120 lbs.

The principal question in deciding between coax and triax lies in the trade-off between weight/diameter advantage of coax and the superior EMI shielding of triax. Assuming the postulated EMI field intensities of 25 volts/meter within the data link passband, and a nominal effective pickup length of 10 meters for the cable exposed at the surface, the typical coax shielding isolation of 110 dB would result in noise levels of about 0.79 millivolts RMS. The received data signal levels, subject to 61.6 dB attenuation in an RG 34B trunk plus the 9.54 dB redundancy allowance, could be as much as 71.14 dB below 20 volts, or 5.55 millivolts peak, which is only 14 dB above the 0.79 millivolt RMS noise. The superior shielding of the triax cable (typically 150 dB) could be expected to improve the 14 dB margin to about 54 dB. A further advantage of the triax for the trunk cable is that it simplifies the transmission of dc power to the ACID by allowing the ac grounded inner shield to carry the positive supply voltage.

(b) Command Transmission Line

To carry the downlink BITE commands from the ACID to the clock module, a trade-off between coax and twisted pair is indicated. The trade-off is highly weighted in favor of the twisted pair, however, since for the audio command frequency of 10 to 20 kHz, either the #19 AWG (0.170 diameter) or #22 AWG (0.160 diameter)

unshielded jacketed twisted pair is quite adequate. As shown in Figure 6-1, the maximum attenuation for these pairs is 0.67 dB/KFT for AWG #19 and 1.15 dB/KFT for AWG #22 at frequencies below 20 kHz. The total attenuation in the 30 KFT run would be 20.1 dB for AWG #19 or 34.5 dB for AWG #22. The command input level necessary at the clock module is 0.15 volts peak, which would necessitate a source amplitude of 1.5 volts for AWG #19 or 7.9 volts for AWG #22.

6.2.1 Attenuation

The attenuation characteristics for the various types and sizes of cables considered in this section are plotted in Figure 6-1 through 6-5. Specific references to the attenuation requirements for the trunk and BITE command functions appear in paragraph 6.2(a) and (b) above. The factors of attenuation affecting the remaining trade-offs are those which apply to the selection of coax versus twisted pair for the 6 mHz clock and the 3 mHz data signals in the array and riser cables.

The maximum allowable attenuation in the clock and data lines in the riser is set by the practical limitation of output from the power boosters driving the riser (2V peak) and the sensitivity attainable at the ACID inputs (100μV peak), which yields a ratio of 86 dB. Allowing 6 dB for semi-failure of the redundant booster outputs, the riser loss is limited to 80 dB, which is equivalent to 8 dB/KFT in the 10,000 foot riser length.

The maximum attenuation permissible in the array clock lines is 18 dB between repeaters, due to constraints in the range of clock input voltages which can be applied to the existing transmitter modules (63 millivolts to 2 volts peak). Although this is a 30 dB range, 6 dB is lost due to the

necessity to operate the clock at 1 volt peak,reserving the 2 volt clock output level for frame and word sync identification. Another 6 dB is lost through the need to allow for semi-failure of the double-redundant clock and clock repeater output stages. The attenuation level permissible in the array data line is greater than for the clock line, since the repeaters can be designed to operate on data input levels as low as 1 millivolt peak. The transmitter module output of 0.5 volts peak, diminished by semi-failure to 0.25 volt, would still allow 48 dB loss from the most distant transmitter driving a repeater. In spite of the fact that attenuation requirements for data are less stringent than those for the clock, cables chosen must be the same for the clock and data lines to preserve their phase tracking. The clock attenuation limits, therefore, effectively restrict the choice of wires or cables to those having less than 8 dB/KFT for the riser and 18 dB between buffers in the array at the clock frequency.

6.2.2 Power Requirements

The clock and data signal amplitudes as set forth in 6.2.1 above are consistent with the capabilities of the existing transmitter hardware and the practical levels obtainable in the new designs, given the optimum dc power distribution system compatible to both.

6.2.3 Number, Types and Sizes of Wire

The types and sizes of wires and cables applicable to the trunk and BITE command lines are discussed in paragraph 6.2.(a) and (b).

The remaining wire comparisons and trade-offs concern the clock and data lines for the riser and array. As detailed in paragraph 6.2.1, the pre-requisite for consideration of any cable for these functions is attenuation

at the clock frequency of less than 8 dB/KFT in the riser and 18 dB between repeaters in the array. Two clock frequencies come under consideration in the trade-off between single and multiple data systems. Since the multiple system is postulated with four channels, the clock rates that apply are 6 mHz for the single system and 1.5 mHz for the multiple system.

6.2.3(a) In the case of the single data system neither of the twisted pairs plotted in Figure 6-2 can meet the riser requirement for 8 dB/KFT at 6 mHz. The AWG #15 size, having 9.1 dB/KFT, would give 91 dB clock loss, or 11 dB more than allowed. Of the RG...U coax cables plotted in Figure 6-3, the smallest diameter class of cables able to meet 8 dB/KFT at 6 mHz is (RG 5, 6, 6A) which gives 6.41 dB/KFT, or 64.1 dB for the total riser. This is 16 dB better than required, but the next smaller size is RG 59, which has 8.4 dB/KFT at 6 mHz and would be 4 dB too high in loss. An ideal (custom made) coax can be projected by the use of the curve of Figure 6-4. By interpolation along the linear slope for 6 mHz it can be found that 8 dB/KFT will correspond to a dielectric O.D. of 0.150 inch. Carrying the d.o.d. value of 0.150 over to the curve of Figure 6-6 yields a projected jacket O.D. of 0.250 inch, and Figure 6-7 likewise yields a projected weight of 300 lbs/KFT. The four cables discussed here are tabulated below with the additional coax RG54A:

	Dielectric O.D.	Jacket O.D.	Atten. dB/KFT	Weight lbs/KFT
AWG 15 pair		0.344	9.1	80.0
RG 59	0.146	0.242	8.4	32.0
Custom	0.150	0.250	8.0	30.0
RG5	0.185	0.332	6.4	88.0
RG54A	0.178	0.250	7.3	27.0

(The jacket O.D. and weight of the RG5 cable are excessive due to a double braid layer, but these values would only drop about 10 percent for single braid.) Note that RG54A is ideal for this particular case in all respects, having a margin of 7 dB when used in the riser. It is an unusual type with a very thin shield, which compromises only performance above 10 mHz for an improvement in size/attenuation ratio at 6 mHz. Note further that the AWG15 twisted pair, though highest in attenuation, is larger and heavier than the four coax types.

For the evaluation of typical cables for application to the array in the 6 mHz (single data system) case, a comparison is given in Table 6-2 of the repeater requirements for various type cables.

	Jacket Diameter		Dielectric Diameter	Atten. dB/KFT	No. of Repeaters	Coax Lbs/ Array
	Sgl Braid	Dbl Braid				
RG 58	.195		.116	9.35	11	1160
RG 59	.242		.146	8.40	10	1280
RG 54A	.250		.178	7.30	9	1060
RG 54	.275		.185	7.30	9	1080
RG 5		.332	.185	6.41	8	3520
RG 9		.420	.280	5.12	6	5600
RG 11	.405		.285	5.00	6	3840
RG 8	.405		.285	4.12	5	4240
RG 14		.545	.370	3.12	4	8640
AWG 15 pair	.344			9.1	11	3200

TABLE 6-2

6.2.3 (b) For the 1.5 mHz clock rate used in the multiple data systems approach, the attenuation requirement of 8 dB/KFT can readily be met with the smallest of the twisted pair or coax cables listed in Figures 6-2 or 6-3. Miniature coax cables such as RG 188, however, have extremely high loss (≈ 40 dB/KFT at 1.5 mHz) and are, therefore, unsuitable. A comparison of RG 122 coax and the AWG 19 shielded pair is given below:

	Jacket Diameter	Atten. dB/KFT	No. of Repeaters	Weight lbs/KFT	Cable lbs/ Array
AWG 19	0.212	7.5	9	27	1890
RG 122	0.160	5.2	6	16	1120

The multiple data system requires an accumulation of data lines along the array such that the total length of the data cable in the array is

$$[(1x6.7) + (2x3.3) + (3x3.3) + (4x6.7)]KFT$$

for a total of 50 KFT. The common clock line adds to this for a total of 70 KFT of cable in the array. The riser, carrying four data lines and one clock line, has a total of 50 KFT of cable.

6.2.4 Repeater Requirements

The repeater requirements for the basic 6 mHz and 1.5 mHz clock rate systems are shown in paragraphs 6.2.3(a) and 6.2.3(b) respectively.

It has been suggested that the repeater requirements might be relaxed by operating at somewhat reduced clock rates, accepting the resulting loss in overall system acoustic bandwidth. The reduction in clock frequency, in effect, reduces cable losses, allowing for the use of fewer repeaters, or smaller diameter cables, or both. Figure 6-9 gives plots of the system audio bandpass as a function of coax cable dielectric diameter for various numbers of repeaters. The dielectric diameter can be converted to jacket diameter by referring to Figure 6-6.

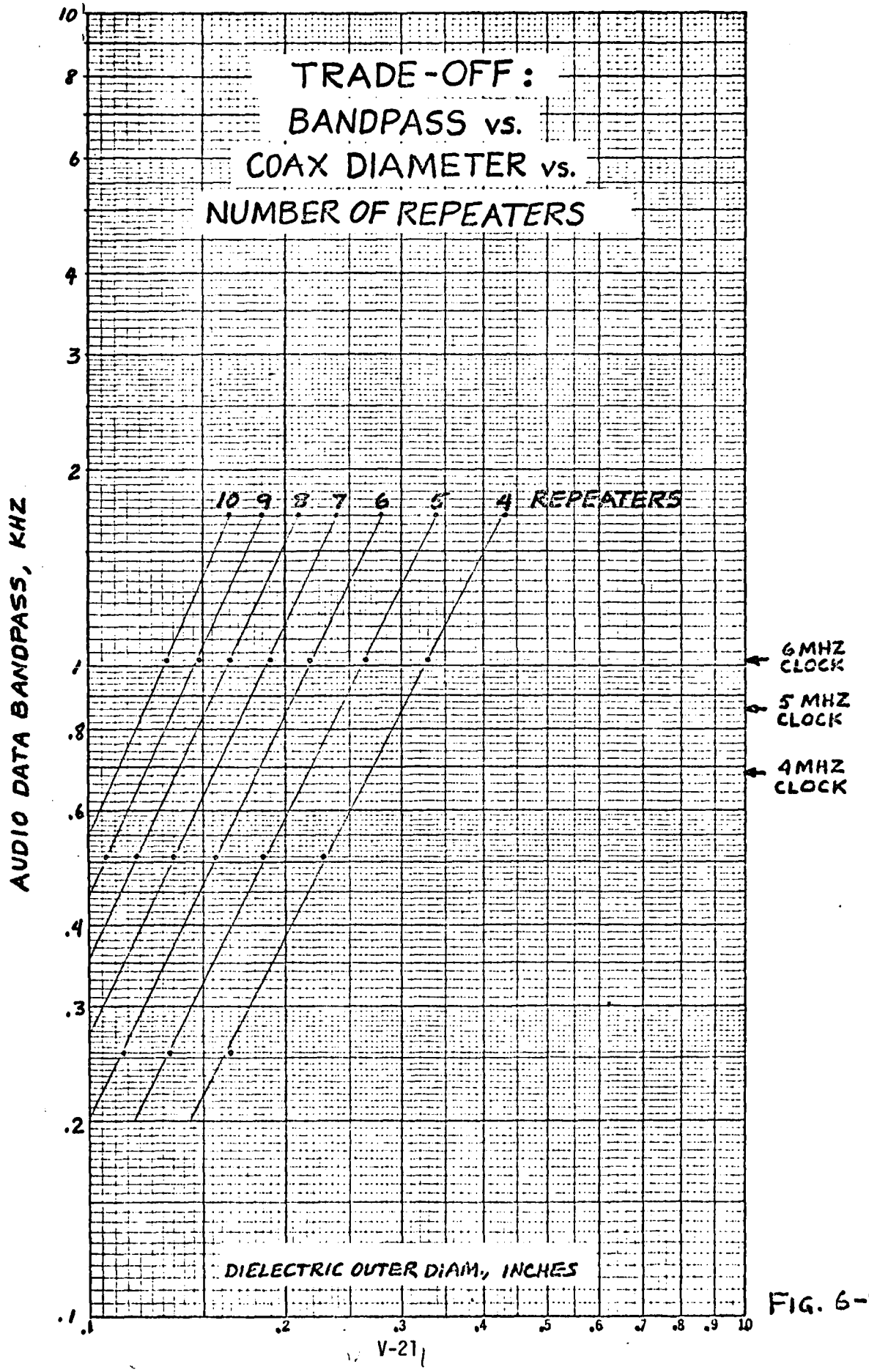

TRADE-OFF:
BANDPASS vs.
COAX DIAMETER vs.
NUMBER OF REPEATERS
AUDIO DATA BANDPASS, KHZ
10
8
6
4
3
2
1
.8
.6
.4
.3
.2
.1
10 9 8 7 6 5 4 REPEATERS
6 MHZ CLOCK
5 MHZ CLOCK
4 MHZ CLOCK
DIELECTRIC OUTER DIAM., INCHES
.1
.2
.3
.4
.5
.6
.7
.8
.9
10

FIG. 6-9

SECTION VI. MODIFICATION OF TLA CIRCUITS

Paragraph numbers are taken from Statement of Work.

5.0 PERFORMANCE/DESIGN OF PRESENT TLA SYSTEM

5.2.1 Phase Tracking 1 to 10 Hz

Reference, 3312237 Preamplifier, Transmitter, Schematic.

A computer analysis was performed for the TLA project to determine worst case phase shift and amplitude variation through the preamplifier. For this analysis R10 was set to 60,000 ohms ±1%. The results are shown on the left hand side of Figure VI-1. The dashed lines show the effect of allowing R10 to vary over the full range shown on the schematic, 54K to 66K. The dashed lines were obtained by hand calculator using equivalent circuits with C1, R10, C5 and R15 as the only significant parameters.

The right hand side of Figure VI-1 shows the ±2.5 sigma limit at $\pm 4^{o}$ of the phase shift measured on eight preamplifiers using a 1000 picrofarad souce impedance. The dashed lines show the calculated worst case combinations of preamplifier parts for a 1000 pf hydrophone and for a 1940 pf hydrophone.

It can be concluded that hydrophone capacitance and sensitivity should be controlled and/or trimmed if phase tracking errors are to be held to less than 5 degrees.

5.2.2 Potential Impact of Changing Clock Frequencies

Capacitors which couple signals at the clock frequency will experience a different attenuation and phase shift when the clock frequency is changed. Capacitors which filter by bypassing square waves of current will have a larger ripple at lower clock frequencies. Capacitors which bypass impulse-type currents will work as well at lower frequencies. Capacitors in analog circuits and power supply circuits are not affected.

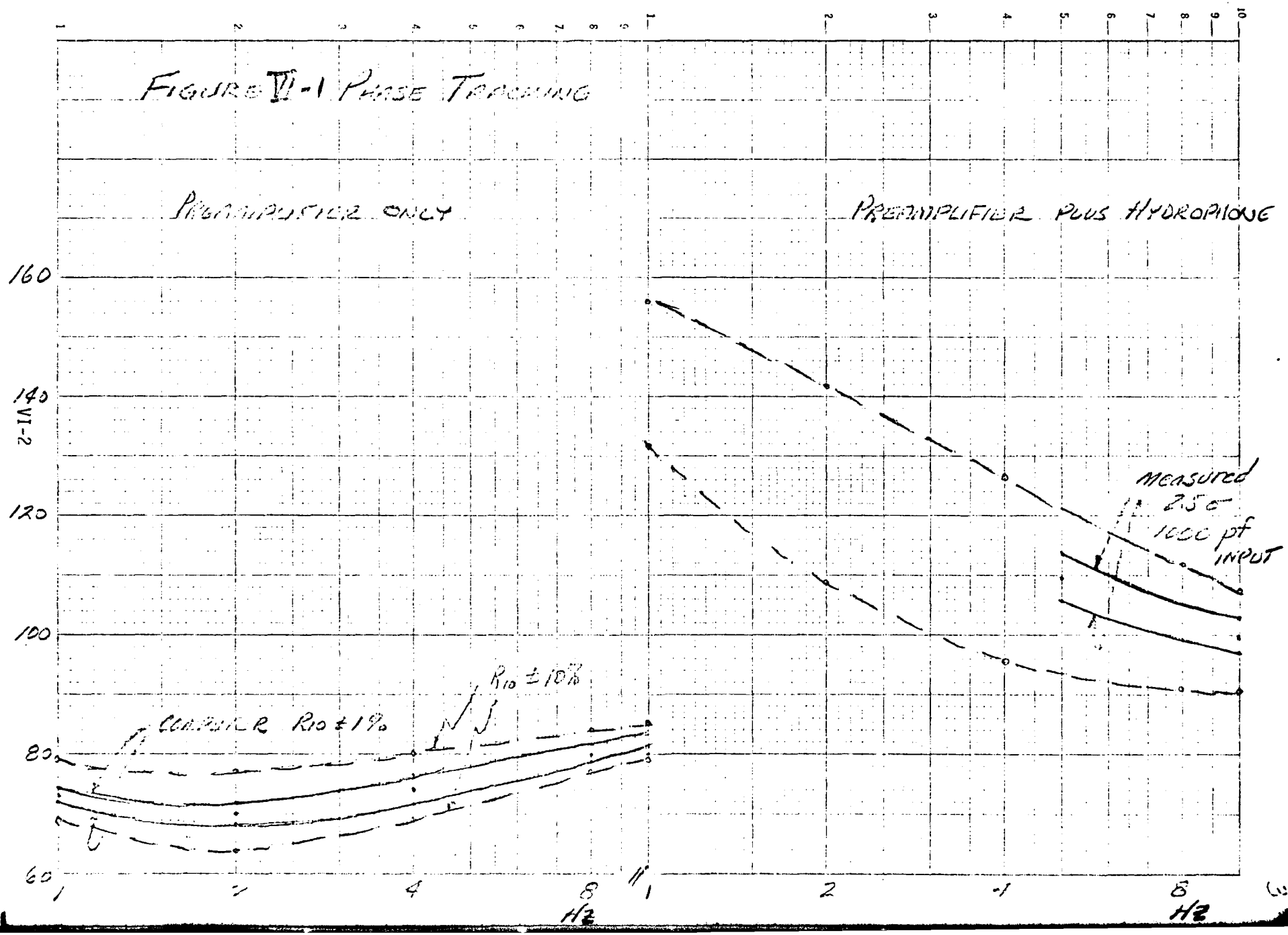


FIGURE VI-1 PHASE TRACKING

The largest capacitors and therefore most significant, are the high voltage capacitors which couple clock and data signals between the array cable and the various units.

C_1 and C_2 on the TLM control couple the clock into the transmitters. Attenuation is negligible at 6, 3 or 1.5 mHz but variations in phase shift result in a slight narrowing of the eye pattern at the receiver.

Since the clock waveform is non-sinusoidal near the clock there is a spread in phase shifts. The RC time constant is on the order of 4 clock periods at 6 mHz. With a square wave input there is no change in phase shift at these frequencies. With a sine wave input (far from clock) the phase shift varies from a theoretical 2.3^{o} at 6 mHz to a theroretical 9.0^{o} at 1.5 mHz (approximately 1-4 ns).

C_9 and C_{10} of TLM Control (each 3300 pf) couple a square wave of current to a 25 ohm load. Near the clock, the current is 20 ma, present design. The change in capacitor voltage is IT/C, or $20 \times 10^{-3} \times \frac{10^{-6}}{12} \times \frac{10^{12}}{3300} = 0.5$ volts in each capacitor. A larger voltage will saturate the driving transistors. There are two solutions at 1.5 mHz, either to quadruple the size of the capacitor or to reduce the data power by 12 dB.

These four capcitors, C_1, C_2, C_9 and C_{10} occupy 5 percent of the substrate area. Doubling capacitance requires 5 percent more area. Quadrupling requires 15 percent more area.

The same size capacitors perform the same function on the data control assembly of clock units.

The two remaining capacitors which couple to the array cables are C_8 and C_9 of the clock control assembly, clock unit. The same reasoning applies.

At lower frequencies either the clock power must be reduced or the capacitor size must be increased. These two capacitors occupy 7.4 percent of the substrate. At the lower frequencies the increase in area is 7.4 percent and 22.2 percent. The clock control substrate is nearly full at present.

In other digital circuits there are ten 12 volt capacitors which could be doubled or quadrupled in capacity without increasing area, and three 2200 pf 12V capacitors which would require an increase in area.

5.2.3 Lowering Transmitter Response

Frequency range - reduce frequency upper limit by 36 percent.

This change permits reducing the sample rate (frame rate) by 36 percent maintaining all other parameters the same. Clock rate would, of course, go down proportionately.

The decrease in upper frequency would require some design attention to maintain rolloff characteristic, so as to keep response aliasing to the present limits when the sample rate is lowered.

As the preamplifier is very dense, significant response changes (downward) would require a major relayout, due to the higher value resistors and/or capacitors required.

Lower clock rate without reducing word or frame length (bits) lowers the signal sample rate, requiring reshaping of the frequency response to maintain present aliasing rejection. Either a faster rollof of upper frequency response, or a lower cutoff frequency would be required. Layout changes of the preamplifier would be required.

5.2.4 Changing Number of Channels per Array

With 1/2 or 1/4 the number of transmitters per frame, the same frame

time, sampling rate and pre-sampling filters could be used with a clock frequency 1/2 or 1/4 of the present value.

5.2.5 Adequacy of Power Supply Regulators

The adequacy of the power supply regulators is evaluated below for the existing design assuming the maximum line voltage is 180 volts at the near end of the array. Changes in the design required by higher voltages will also be indicated.

If the line voltage applied to a string of transmitters varies from 96 to 180 volts due to IR drop, the voltage applied to a transmitter power supply varies from 16 to 33 volts, with six transmitters in a string. The variation in voltage will be absorbed across R8 and the collector of Q2, and possibly across the 33 volt zener. The dynamic resistance of each unit varies from approximately 1000 ohms to approximately 1630 ohms with 32 volts across the unit.

The thermal resistance for each component of the regulators was calculated, from surface of the part to bottom of substrate. The temperature rise for each part was calculated for the nominal case (20 volts, 60 ma). Thermal resistances are given in Table VI-1 and nominal temperature rises are given in Table VI-2. Figure VI-2 shows the nominal circuit.

The voltage-current regulation characteristic was calculated for Q1, Q2 junction temperature of 0^{o} and 40^{o}. The temperature rise for R8 and Q2 was calculated for the assumption that the junctions are maintained at 0^{o} and 40^{o}. This would require an adjustment of the temperature of the bottom of the substrate. (In actuality the temperature rise of R8 will heat the junction of Q1, causing more voltage to be applied to the unit.)

TABLE VI-1

THERMAL RESISTANCE

Sch	Comp.	Approx. Area (mils)	Eff. Substrate Area (mils)	Bond	Sil	Bond	Subs	°C/W Total
3312227	Q1	20x20	60x60	Cond. Epoxy	11.7	49.0	10.9	71.6
	Q2	30x30	70x70	Eu	5.2	0	8.0	13.2
	VR1	30x30	70x70	Cond. Epoxy	5.2	21.8	8.0	35.0
	VR2	25x25	65x65	Eu	7.5	0	9.3	16.8
	R7	12x20	52x60	Cond. Epoxy	19.5	81.8	12.6	113.9
	R8	4x28	44x68	Cond. Epoxy	42.8	175.2	13.1	231.1
	R9	4x142	44x182	Cond. Epoxy	8.3	34.5	4.9	47.7
3312237	VR1	35x35	75x75	Cond. Epoxy	3.8	16.0	7.0	26.8
	VR2	35x35	75x75	Cond. Epoxy	3.8	16.0	7.0	26.8

TABLE VI-2

Typical Power Dissipation and Temperature Rise

Trimmed to 20 volts and 60 ma
Currents estimated from best available data

Component		Power Dissipation		Th Res.	Temperature Rise
	Q1	4 ma 1.35 V	5.4 mw	71.6°C/W	0.4°C
	Q2	56 ma 4.3 V	240.8 mw	13.2	3.2
	VR1	13 ma 10 V	130 mw	35.0	4.6
	VR2	- (35 V)	-	16.8	-
	R7	15 ma 4V	60 mw	113.9	6.8
	R8	4 ma 8.65V	34.6 mw	231.1	8.0
	R9	56 ma 0.7 V	39.2 mw	47.7	1.9
Preamp	VR1	40 ma 5V	200 mw	26.8	5.4
Preamp	VR2	10 ma 6V	60 mw	26.8	1.6

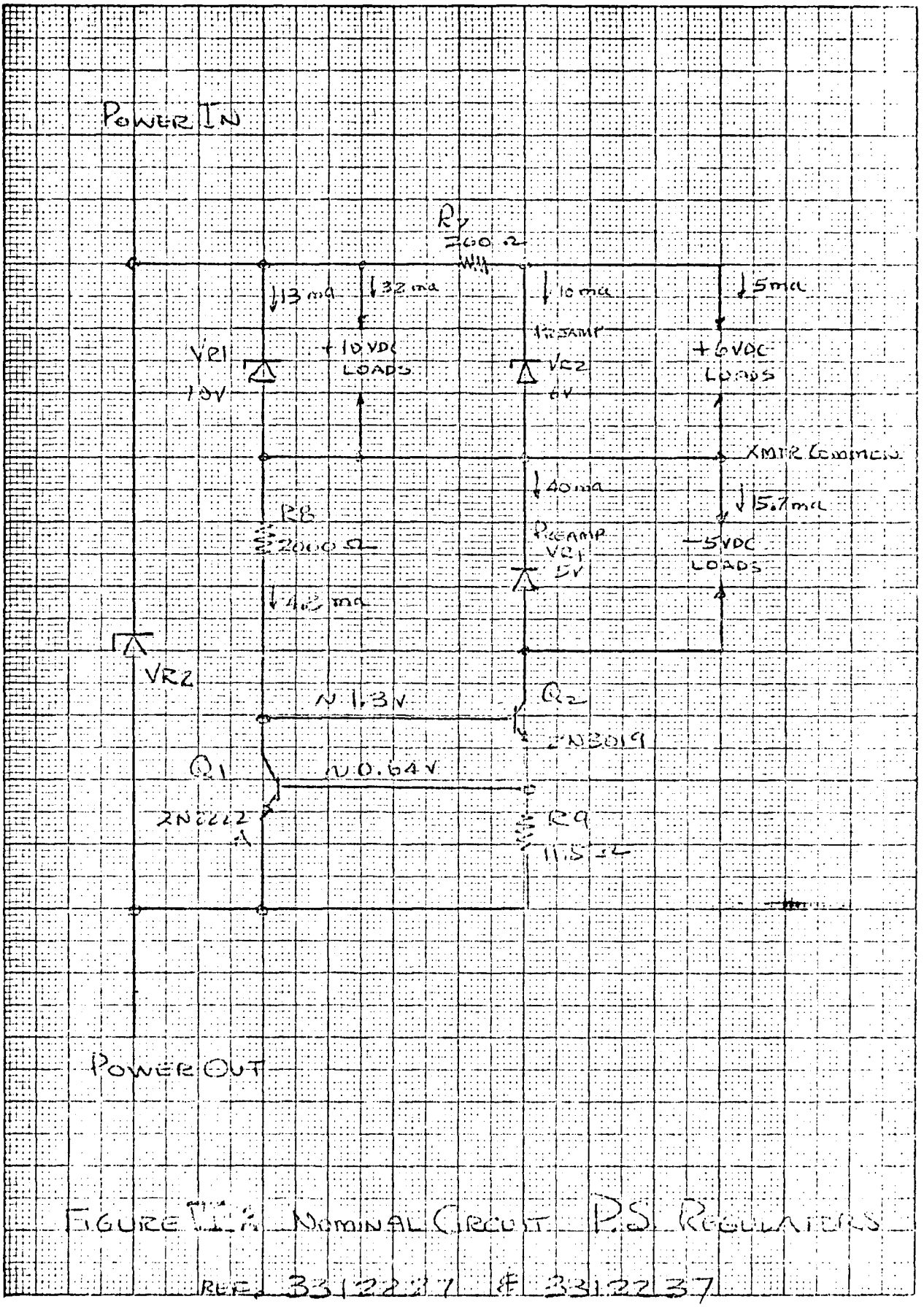


FIGURE VI-2 NOMINAL CIRCUIT PS REGULATORS

REF. 331223-1 & 331223-2

These curves are shown in Figure VI-3. From the V-I curve, at currents greater than 62.5 ma and less than 66.5 ma, a junction temperature change of $40^{o}C$ is equivalent to 10 additional volts across the unit, or $4^{o}C$/volt. From the lower curves, the ten volt change causes the R8 temperature rise to change 28^{o} to 44^{o} or $2.8^{o}C$/volt at 62.5 ma and $4.4^{o}C$/volt at 66.5 ma. Since the thermal coupling between R8 and Q1 is less than one, the thermal loop gain is never unity, but it is clear that the hotter circuits will absorb more voltage. This process is limited at 33 volts at the high end and 62.5 ma at the low end, so there is no danger of pushing a cold unit out of regulation. The regulator characteristics were obtained by fitting National Semiconductor curves for base-to-emitter voltage (typical) with

$$V_{be} = 0.65 + 0.065 \log i_c - .0022\ T \text{ for the 2N2222A and}$$

$$V_{be} = 0.62 + 0.050 \log i_c - .0018\ T \text{ for the 2N3019,}$$

where i_c, collector current, is in milliamperes and T is in ^{o}C.

The 33 volt zener limits the maximum voltage absorbed by a unit and in the event of a transmitter failure assures that current will be furnished to the remaining transmitter units in the string. If a transmitter load fails open with a line voltage of 180 volts its 33 volt zener will experience its worst case temperature rise. The voltage across the ramining units has an average value of 29.4 volts. Suppose two of the higher resistance units increase in temperature until their 33 volt zener conducts a small current. The voltage across the three colder units would then become

$$\frac{180 - 3(33)}{3} = 27.0 \text{ volts}$$

This would require Q1 of the hotter units to be $24^{o}C$ hotter than Q1 of the colder units (from V-I curves of Figure VI-3). The maximum string current

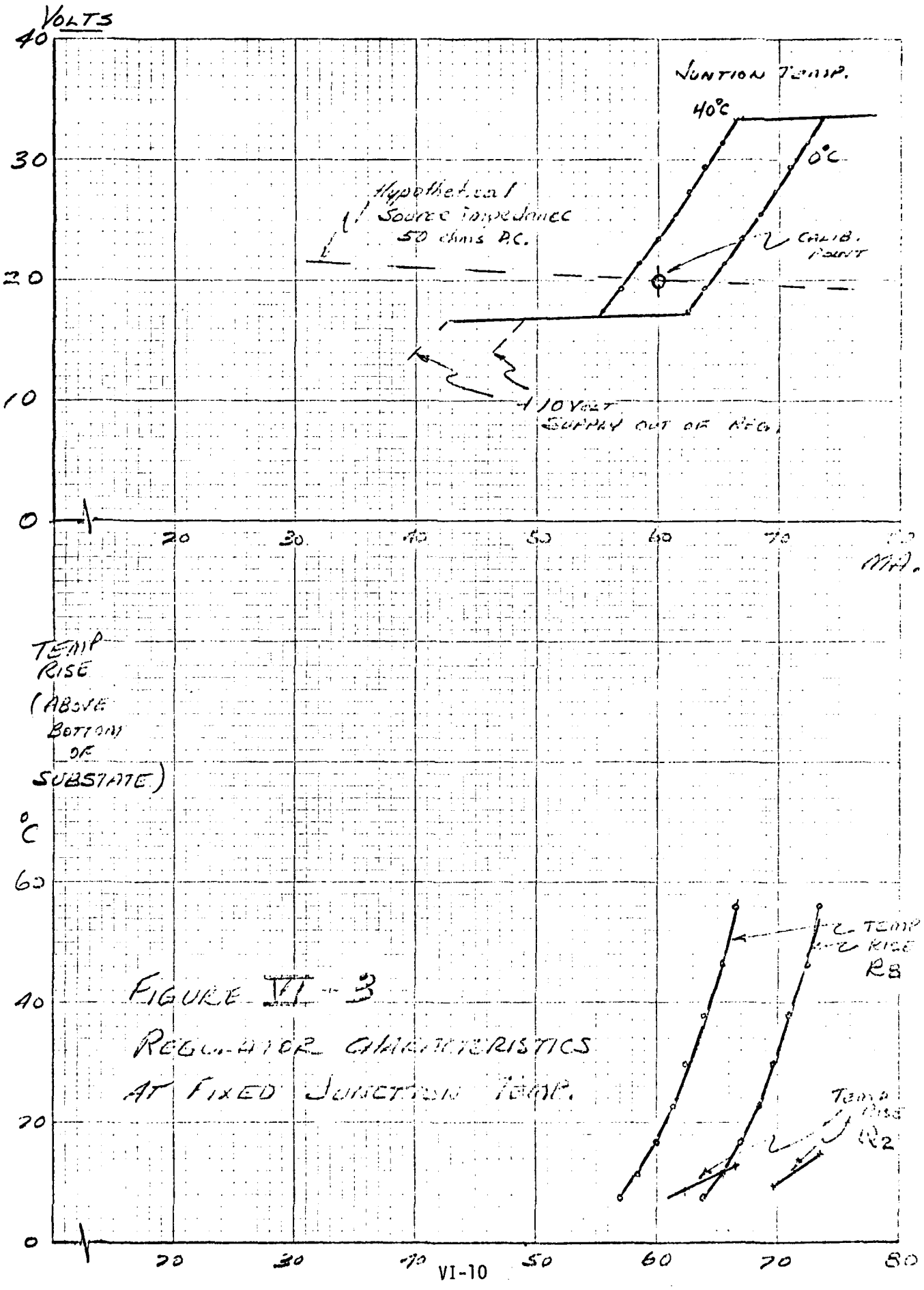


FIGURE VI - 3

REGULATOR CHARACTERISTICS AT FIXED JUNCTION TEMP.

would be 65 ma at a core temperature of $0^{o}C$, with smaller currents at higher core temperature. From the T-I curves of Figure VI-3, R8 has a temperature rise of 40^{o} at this current and Q1 temperature rise will be less than $20^{o}C$. 65 ma will be the worst case current through the 33 volt zener of a failed unit. With a core temperature of $0^{o}C$, a dissipation of 0.065 x 33 = 2.14 watts, a thermal resistance of $\frac{16.8^{o}C}{W}$, the temperature rise of VR2 is $36^{o}C$. With a core temperature of $40^{o}C$ the current is about 60 ma, the temperature of Q1 of the cold units is about 50 to 52 degrees, and the temperature rise of VR2 in the failed unit is 0.060 x 33 x 16.8 = $33^{o}C$.

These calculations indicate that the existing power supply design will be adequate for line voltages between 96 and 180 volts.

If it is necessary for transmitter strings nearest the power source to experience line voltages greater than 180 volts, it will then be necessary to change the zener voltage of VR2 to a value greater than 33 volts, to increase the voltage rating of the capacitors which couple clocks and data signals to the array and to increase the maximum dissipation in R8 and in Q2. If the temperature rise in R8 is allowed to become $135^{o}C$, the power dissipated in this resistor will be on the order of 580 milliwatts.

Q1 is located 60 mils from R8 and the substrate is 20 mils thick. The heat rays from R8 will be curved toward the cold surface of the substrate. The isotherms from R8 will be approximately long cylinders. If the cylindrical surface 20 mils from R8 transmits W watts the surface 60 mils from R8 transmits less than W/3 watts. The temperature rise of Q1 due to heat in R8 (on this basis) is less than 1/3 the temperature rise in R8. For a

simplified worst case assume the rays are straight lines and the rise in Q1 is therefore 1/3 the rise in R8 (plus internal rise).

The temperature rise of Q1 will be approximately $(135/3+1.4) \approx 47^{o}C$. The base-to-emitter voltage of Q1 will drop (0.0022) (47) = 0.103 volts. The current through R9 and Q2 therefore suffers a delta of 0.103/11.5 = 9.0 ma. The increase in current in R8 at $135^{o}C$ is 17 ma, and the voltage across R8 will be 34 volts. The decrease in current through R9 appears externally as an increased dynamic resistance. The voltage across a transmitter will be 45.3 volts, and allowing a 10 percent safety margin, the maximum line voltage will be 45.3 x 6 x 0.9 = 244 volts. By changing the shunting zener from 33 to 45 volts, higher voltages could be applied to a string.

5.2.6 256 Channel D to A Conversion

The options used in going from bit-serial digital data to 256 parallel analog channels involve the cost and size of DACs and sample-and-hold circuits which have various settling times. The make-or-buy option is considered out-of-scope.

Letting N take on the values 1, 2, 4, 8, 16 - - - etc., let the DAC equipment consist of N 8-bit storage registers, each holding successive words for N word-times, N digital-to-analog converters, sample-and-hold circuits which store each word at conversion time, 256 sample-and-hold circuits which re-sample simultaneously at the end of each frame, the digital equipment required to generate loading, conversion and sampling gates and 256 analog filters which attenuate sum and difference frequencies or sidebands at each harmonic of the sampling frequency, in order to restore the base band waveform.

It is conceivable that the conversion time sample-and-holds could operate sequentially, à la bucket brigade, which would simplify the sampling gate hardware; however, the speed and accuracy of the sample-and-hold makes cost prohibitive. The conversion time sample-and-holds therefore consist of N groups of 256/N S & H's connected in parallel, each group being supplied by one of the N DAC's. Cost and size therefore are a function of N only. The parts characteristics to be traded are tabulated below.

TABLE VI-3

Components	Approximate Settling Time	Approximate Size	Estimated Relative Parts Cost/Channel	Function
LH0032 T08 2N4381 T018 LH0033 T08 9 discretes	0.5 μsec	2.5 sq.in.	160	S&H
LH0053 T08 1 discrete	2.0 μsec	0.6 sq.in.	60	S&H
CA3080E T05 3N138 T072 6 discretes	14.0 μsec	1.0 sq.in.	20	S&H
(2) AD7520 (2) LH0024 + Logic	0.7 μsec	6.0 sq.in.	320	DAC
(2) AD7520 (2) LH0003 + Logic	2.0 μsec	6.0 sq.in.	200	DAC
MSI TTL CHIP			8	Control
SSI TTL CHIP			1	Control
Bipolar PROM's			68	Control

Combining costs and sizes, Figure VI-4 shows relative cost and size for several different configurations. Unity relative cost does not include non-recurring cost and does not include cost of 256 analog filters or printed circuit boards. Non-recurring cost should not be affected by N. Unit size is 630 square inches.

The minimum cost configuration consists of 2 cards for timing logic, sixteen identical DAC cards, and 16 identical analog filter cards.

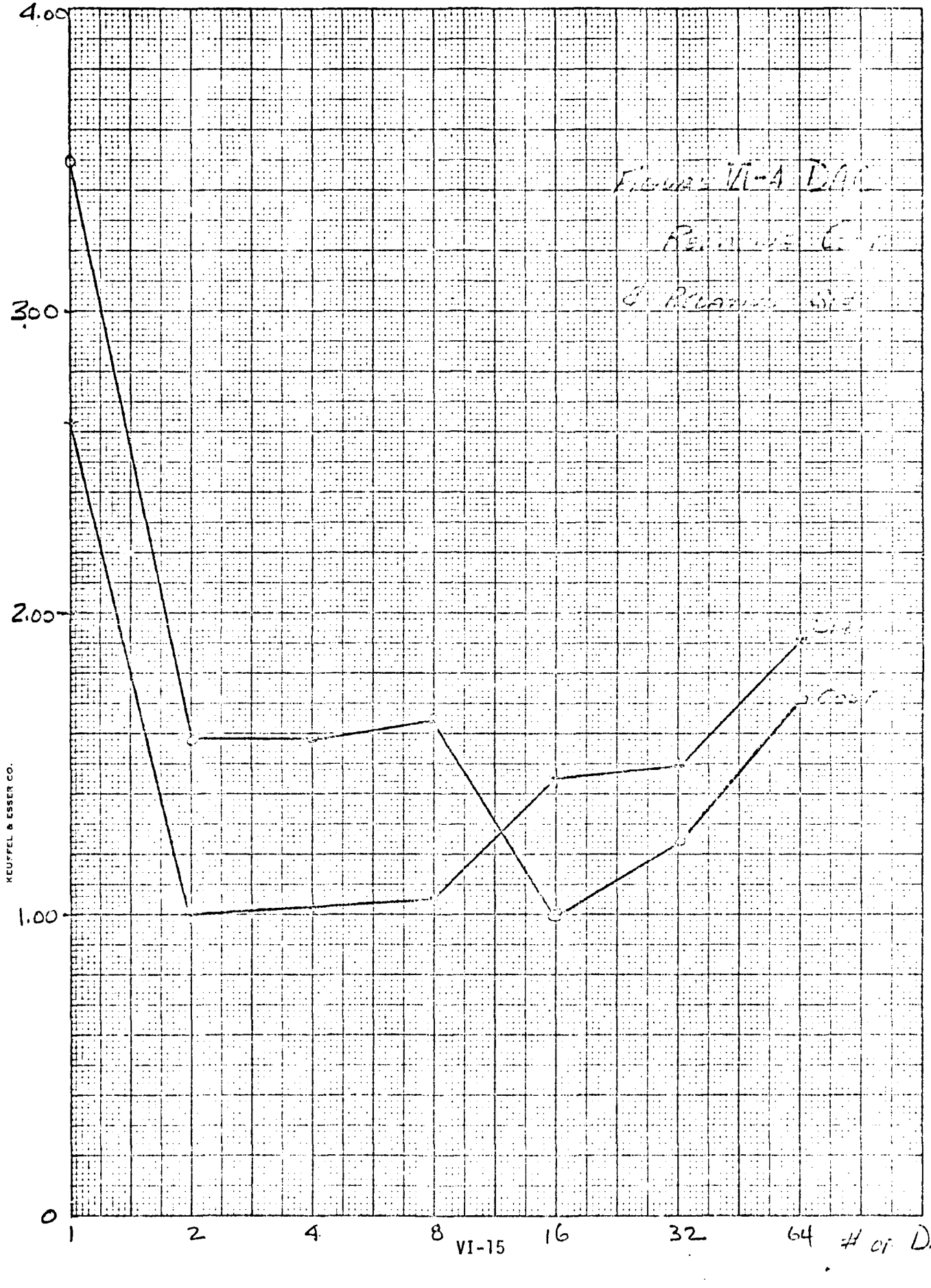
Each DAC assembly has an eight-bit buffer register, a word counter (÷16 operated by word clock), a DAC, 16 "conversion complete" sample-and-hold circuits, and 16 resampling sample-and-hold circuits, operated at frame time. Each DAC card requires approximately 35 square inches and has 31 (plus spares) pins.

Analog filters are required to restore the original waveform. The number of poles required depends upon the sensitivity of the beamformer to the sampling distortion. If steep filters are required, 16 more cards, each containing 16 filters will be used.

5.2.6.1 2's Complement Form 12 Bits

The existing TLA receiver converts the eight-bit telemetry code to a 13-bit 2's complement code via bipolar PROMS.

The existing transmitter can be used to generate a 12-bit 2's complement code by detecting all outputs whose magnitude is greater than 2047 (telemetry code x 111 XXXX) and setting these numbers equal to ±2047, 0 111 1111 1111 or 1000 0000 0001. This change can be effected by reprogramming the PROM's.


4.00
3.00
2.00
1.00
0
1
2
4
8
16
32
64
# of DACs

The effect of truncating the existing telemetry code at ±2047 can be evaluated by considering Figure VI-5.

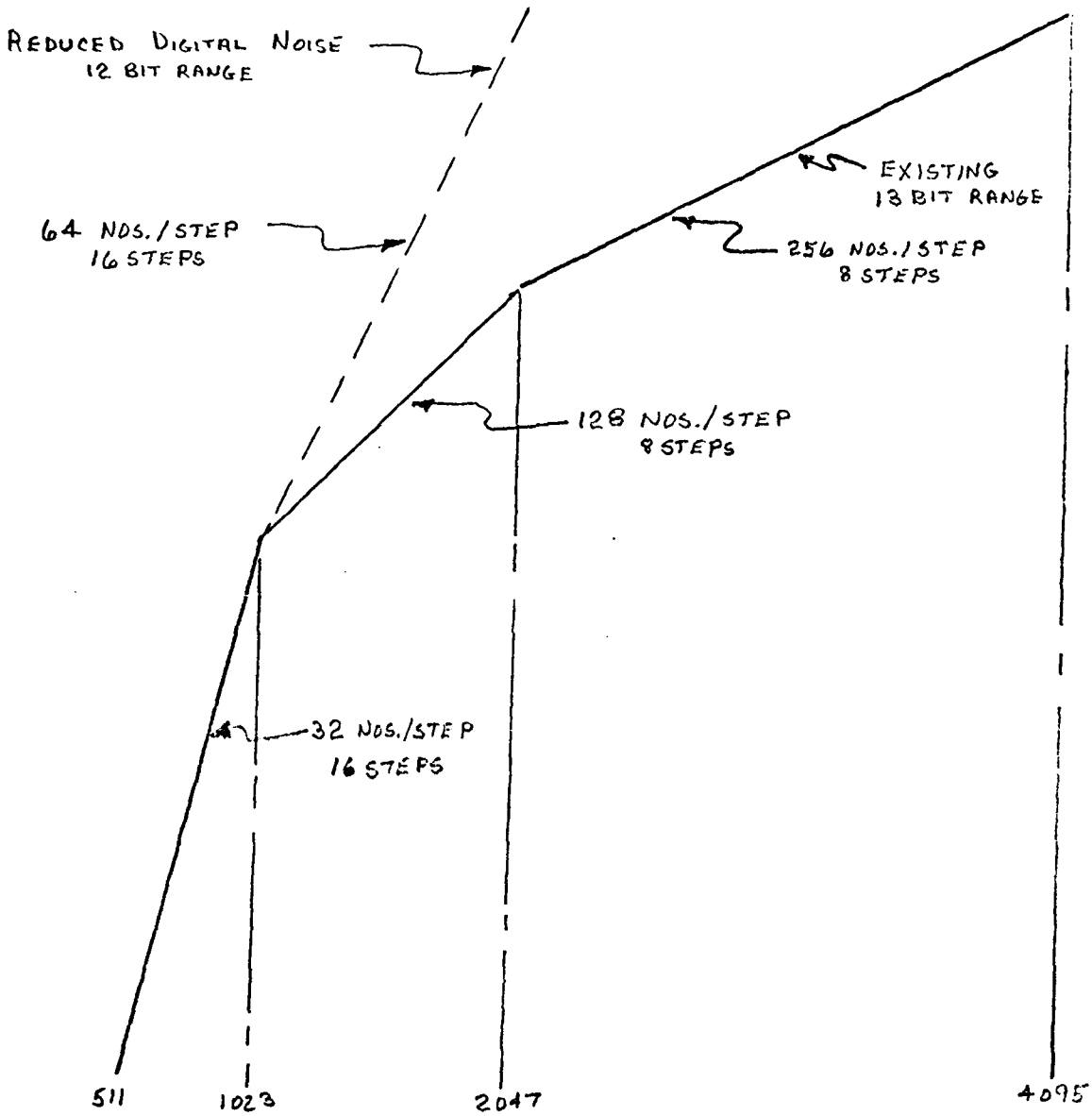


FIGURE VI-5

The solid line in Figure VI-5 shows the existing 8 bit/13 bit coding. Setting numbers greater than 2047 equal to 2047 results in a loss of 6 dB in the theoretically ultimate dynamic range. This loss is inevitable in going from a 13 bit to a 12 bit code.

Only eight steps are available from 1023 to 2047. Modifying the transmitter would result in a reduction in digital noise in this range, since 16 steps could be used. A code which could be used is shown in Table VI-4.

Transmitter modification required to achieve the reduction in digital noise possible consist of grounding the MSB input to U3 (3312227) and eliminating the AND/OR SELECT gate U9, so that 16 bit resolution is obtained for every scaling range.

The amount of reduction in digital noise depends upon the scaling and distribution of the signal. Referring to Figure VI-5 if the signal lies between 1023 and 2047 most of the time then the digital noise can be reduced by 6 dB since the error can be reduced from sawtooths with a peak of ±64 LSB's, to sawtooths with a peak of ±32 LSB's. If the signal comes from a large number of small sources and 2047 corresponds to the 2-sigma level, then the peak digital error has the following distribution.

TABLE VI-5

Percent	Range	Peak Error	
		Unmodified	Modified
.197	Less than .25 sigma	4 or less LSB's	4 or less LSB's
.186	.25 to .50	8	8 LSB's
.300	.50 to 1.0	16	16
.272	1.0 to 2.0	64	32

TABLE VI-4

No.	Telemetry A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	12 bit 2's Complement b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	LSB's Step
+2047	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	
1087	1	1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	1	64
1023	1	1	1	0	1	1	1	1	0	0	1	0	0	0	0	1	1	1	1	1	
543	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	32
511	1	1	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	
271	1	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	16
255	1	1	0	0	1	1	1	1	0	0	0	0	1	1	1	1	1	1	1	1	
135	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	8
127	1	0	1	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	
67	1	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	4
63	1	0	1	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	
33	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	2
31	1	0	0	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	
16	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	
15	1	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1
+ 1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	
0									0												
- 1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	
15	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	
16	0	0	0	1	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	
31	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1	
33	0	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	1	1	1	1	
63	0	0	1	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	
67	0	0	1	1	0	0	0	0	1	1	1	1	1	0	1	1	1	1	0	1	
127	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	
135	0	1	0	0	0	0	0	0	1	1	1	1	0	1	1	1	1	0	0	1	
255	0	1	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	
271	0	1	0	1	0	0	0	0	1	1	1	0	1	1	1	1	0	0	0	1	
511	0	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	
[illegible]	0	1	1	0	0	0	0	0	1	1	0	1	1	1	1	0	0	0	0	1	
	0	1	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	
	0	1	1	1	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	1	
			1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	

Resolution Bits

Resolution Bits

Digital error, unmodified system,

$$\left[\frac{.272}{3}(64)^2 + \frac{.300}{3}(16)^2 + \frac{.186}{3}(8)^2 + \frac{.197}{3}(4)^2\right]^{1/2} \leq 20.0 \text{ LSB's}$$

Digital error modified system

$$\left[\frac{.272}{3}(32)^2 + \frac{.300}{3}(16)^2 + \frac{.186}{3}(8)^2 + \frac{.197}{3}(4)^2\right]^{1/2} \leq 11.1 \text{ LSB's}$$

For this signal, the improvement is 5.1 dB.

5.2.7 Mechanical Design Modifications

5.2.8 External Addressing

See Section II-e above.

5.2.9 Recording of Telemetry Data

The telemetry data can be recorded as eight-bit words, together with a 750 kHz word clock, in nine channels of a tape recorder. The existing receiver design can be used to establish word sync, and to load the 8-bit words into a buffer register for recording.

On playback, the data are handled as 8-bit words, therefore, all of the timing waveforms required can be derived from the one clock recorded.

If a tenth channel is available, the frame sync pulse can also be recorded. Alternatively, three parallel-in parallel-out 8-bit storage registers can be used to store three successive words, and with proper decoding, the frame sync pulse can be reconstructed to re-establish channel identification.

Fairly minor changes are required to use either the recorded clock for word processing, or to use the word clock derived directly from the uplink, as in the existing design.

It is entirely feasible to build a receiver which can be switched at will from live data to the recorded data described above.

The existing receiver design will not interface directly with a digital computer unless the computer has I/O equipment capable of handling a continuous data stream, specifically 13 (12) bit 2's complement data and an eight-bit channel identification number, or address, at a 750 kHz word rate.

A buffer memory could be designed and built to store the data in large blocks for the most economical computer useage, but the specifications and requirement are not known at present.

If only eight channels are available for recording telemetry data it is not necessary to record a word clock. Bit transitions can be detected by limiting, differentiating, rectifying and summing the 8 transitions together. A phase-lock loop can be used to take care of the possibility that all eight bits are the same in two successive words. Additional hardware is required. Recording of nine or ten channels is preferable if nine or ten channels are available.

SECTION VII. CALIBRATION AND COMMAND SYSTEM

4.0 CALIBRATION/COMMAND SYSTEM

4.1 CALIBRATION SIGNAL STUDY

4.1.1 Noise Source

The noise sources considered are noise diodes and digital pseudo-random sequence generators. The noise diodes, buffered by an amplifier with approximately 32 dB of gain, is a small and relatively economical solution, and would permit a check on the frequency response of the preamplifier. This source, however, is not fixed in amplitude and does not permit a check on coherence.

The digital generator can be synchronized, with each transmitter calibrated with identical signals, and the calibration spectrum can be designed to cover enough frequencies and amplitude levels to permit as complete a check on preamplifier and A/D converter as is desired.

Assuming the maximum-length sequence from an N-bit shift register, the sequence is periodic in 2^n-1 bit periods. With a shift clock frequency, fc, the spectrum has lines at $\frac{fc}{2^n-1}$ Hz. The envelope of the lines at the register output has the shape of the spectrum of a single bit, sin x/x, where $x = \pi f/fc$.

The digital level changes are 60 dB greater than the level required at the hydrophone. If the shift clock frequency is high enough, the shift register output could be used without D/A conversion by passing this signal through a low-pass filter. The amplitude of the calibration signal for this approach would depend upon the stability of the low frequency corner.

A calibration signal with a more accurate amplitude is obtained by using m successive bits of the sequence to operate a ladder network. The envelope of

the line spectrum for this approach is sin y/y, with $y = \frac{m\pi f}{f_c}$.

In order to exercise the full bandwidth of the preamplifier, the calibration signal spectrum should have substantial values throughout the bandpass. This will be achieved if the first null of sin x/x or syn y/y is at the sampling frequency or higher.

$$\frac{2930}{\pi x 1020} \sin \frac{\pi 1020}{2930} = 0.812$$

Stepping the input at the frame rate will cause lines at 1020 Hz to be down 1.8 dB relative to low frequency but this would become a known correction to be applied.

A convenient shift clock, already existing, is the Q_8 output of the SAR clock counter. The frequency at this point is 6 mHz x 2^{-11} or 2930 Hz (once per frame). A nine-bit shift register, with exclusive - OR feedback from the 5th and 9th stages, would produce lines at 5.73 Hz separations.

4.1.2 Single or Multi-Frequency Source

The existing BITE signal has components at 374 and 1122 Hz which can be measured at the receiver to detect a large percentage of the changes in the preamplifier characteristic which might conceivably occur.

A larger number of frequencies would permit analysis of any such change, and possibly compensation, which would reduce any data degradation. The pseudo-random noise generator is a pre-programmed multiple frequency source which would permit more accurate calibration, but which requires additional hardware.

Other multiple frequency digital signal sources can be developed. The 2930 Hz clock could be used to operate an 8-bit counter, the counter bits being connected to an 8-bit ladder network, the resulting sawtooth being

attenuated and applied to the hydrophone return. This sawtooth has a frequency of 11.45 Hz. The spectrum has lines at 11.45 Hz separations and the envelope has a 1/f characteristic, as can be seen by referring to Figure VII-1.

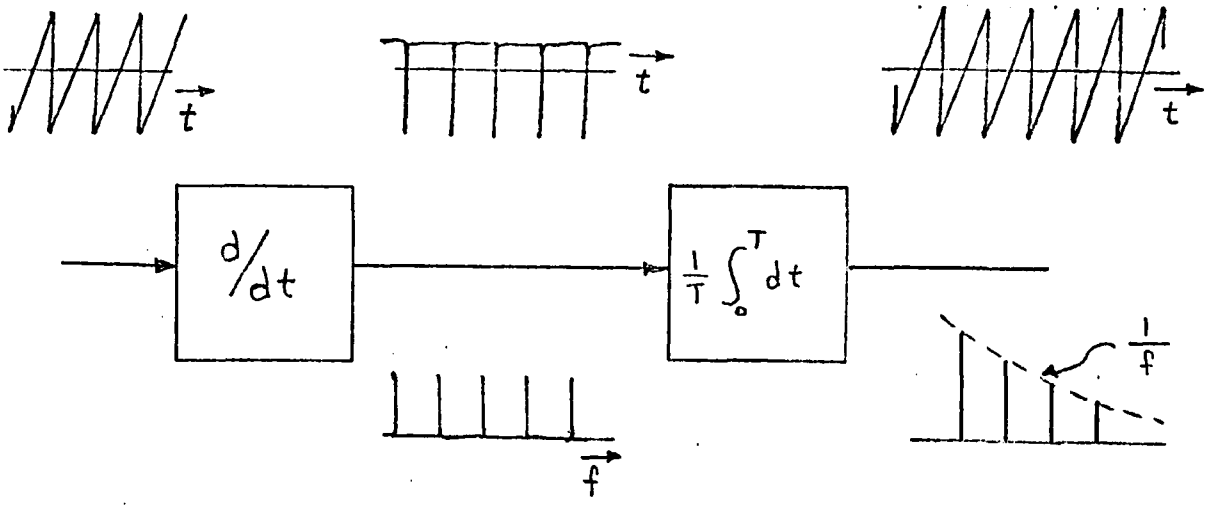


FIGURE VII-1. RAMP WAVEFORM ANALYSIS

The differentiator and integrator are postulated only for the sake of quick analysis and are assumed perfect. The comb-in-time has a comb spectrum and the sawtooth spectrum, therefore, goes as 1/f. This is in contrast to the triangular wave which goes as $1/f^2$, and the pseudo-random digital sequence which goes as sin f/f. Figure VII-1 shows why sawtooth signals are probably not suitable for testing the presampling filter, which has some of the characteristics of a differentiator, followed by a zonal filter. The output of the filter would be a band limited comb function. One frame in 256 would have the task of transmitting the leading edge, or impulse, the remaining

255 would transmit a small dc value corresponding to the slope, plus the zonal filter ripples. A triangular calibration waveform should look something like a square wave, band-limited, at the ADC. Neither of these waveforms will exercise the ADC as much as the pseudo-random waveform.

4.1.3 Coherence of Calibration Signal

The first frame sync signal following the generation of the calibration command can be used to reset and enable the calibration signal generator. All such calibration signals will be coherent.

4.1.4 Switch Dummy Capacitor

A command can be implemented which disconnects the hydrophone, and substitutes a dummy capacitor, in order to permit the observation of the self-noise of a channel. Impact is discussed below.

4.2 IMPLEMENTATION STUDY

The various methods of obtaining a calibration signal are ranked below.

TABLE VII-1. RANKING OF CALIBRATION SOURCES

Method	Cost	Power	Size	Coherent	Freq. Char.	Ampl Char.
1. Noise Diode	2	1	1	No	1	3
2. 23 kHz Shift Clock 9-bit shift register 2344 Hz Analog Filter (Pseudo R)	4	2	2	Yes	3	2
3. 2930 Hz shift clock 9-bit shift register 12-bit ladder network Pseudo-random	5	3	3	Yes	2	1
4. 2930 Hz clock 8-bit counter 8-bit ladder (sawtooth)	3	3	4	Yes	5	1
5. 2930 Hz clock 8-bit Up-Down Ctr 8 bit ladder (triangular wave)	4	3	4	Yes	4	1
6. 374 Hz Square wave (existing design)	1	1	1	Yes	6	1

Table VII-1 gives the rational for current recommendation. The existing design (method 6) is the best on all counts except for bandwidth. Lack of bandwidth is the reascn for considering alternatives. Methods 4 and 5 are not much better in the spectrum department. Method 1 has the best spectrum but is ruled out because it is not coherent and its amplitude will drift. Of the two remaining methods, method 3 has the edge in spectrum and amplitude stability and is, therefore, the recommended method.

4.3 COMMAND TECHNIQUE STUDY

4.3.1 Clock Frequency

Change of clock frequency by command is not recommended, since compatible configuration changes are too extensive to be executed by command.

4.3.2 BITE

BITE is commanded on by applying a suitable clock (see Paragraphs 4.1.1 through 4.2) to a shift register, removing a "set" signal from this register, and applying the output of a ladder network to the hydrophone return via a FET switch and attenuating resistor networks.

4.3.3 Gain

Preamplifier gain can be changed by shunting R10 in the preamplifier by a resistor of equal value. The second resistor can be inserted or removed by means of a FET switch.

4.3.4 Backup Clock

The method of selecting the clock unit in the TLA system can be adapted to stored mode commands in the SEAGUARD system.

4.3.5 Dummy Capacitor

A pair of FET switches can be used to select either "HYDROPHONE INPUT NO. 1" or the high side of a dummy capacitor. The low side of the dummy is connected to "HYDROPHONE INPUT NO. 2".

4.3.6 Underlying Requirements

Regardless of the command technique selected, it is assumed that the status of the array must be transmitted to the receiver. The single status bit in the TLA format will become four status bits.

(a) Main clock - backup clock.

(b) Hydrophone - dummy capacitor.

(c) Calibration On - Calibration Off.

(d) Gain High - Gain Low.

It is assumed that the command system operation and the array status should be immediately evident to the operator. Dual pushbuttons, mechanically interlocked, with the latched depression indicating command, and the illuminated half indicating array status, appears to be a desireable way of monitoring system operations. Using three more status bits reduced the 23-bit sync pattern to a 20 bit pattern, but this is more than ample, for the TLA receiver. During acquisition, the receiver watches for the sync pattern and sets up a time window 23 bits (20 bits) long when it occurs. As long as the sync pattern reappears in this window on each frame, sync is maintained. If the 23 bit (20 bit) pattern is not correct two frames in a row, then sync is lost, and the system opens the window, reverting to the acquisition mode. On power turn-on, or on loss of sync, the probability of 20 adjacent random bits assuming the sync pattern is 2^{-20}. There are 250 x 8 such opportunities in each frame. One re-acquisition (or turn-on) out of 524 will be delayed for two frame times because the random data sets up a false window. This is an insignificant loss. (With a 23-bit pattern, a false window occurs once in 4192 acquisitions.)

The data and clock to the receiver share a common path with command signals to the array. The Array-Cable Interface filters and channels frequencies above a certain value to the receiver as data and clock, and channels frequencies below this value to the array as commands. Command link delays of hundreds of milliseconds would not be a problem since the commands are initiated by human operators. Therefore, very little bandwidth is required by the command channel to satisfy external requirements. The actual bandwidth used will be

determined by array constraints on power, size and simplicity.

4.3.7 Options on Command Modulation Scheme

The modulation scheme for the station - ACID link is not necessarily the same as it is for the ACID-clock unit link or for the clock unit-transmitter unit link or for the ACID-transmitter unit link. It is not necessary for all of these possible links to be present.

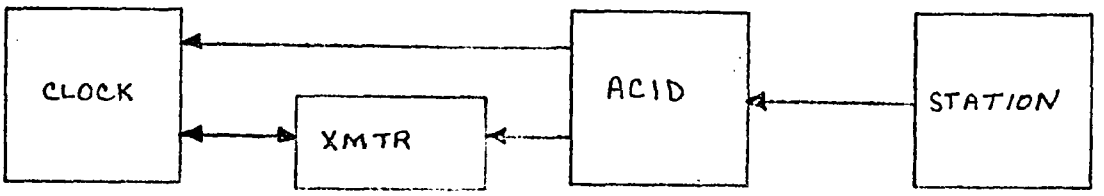


FIGURE VII-2. POSSIBLE COMMAND FLOW

One of the commands, MAIN/BACKUP, operates only on clock units. The other three commands operate only on transmitter units, but the transmitter status is reported by the clock unit, since that is where the sync code pattern, including status bits, is generated. A single chain of command appears desireable, for simplicity, and to improve the likelyhood that all transmitters are in the same mode.

The command link equipment in the ACID should be as simple as possible to improve reliability.

The command link recommended, therefore, has two parts, one from station to clocks, through ACID, and one from clocks to transmitters.

Three approaches are considered for the station-clock link. These are:

(a) Single frequency -time modulated.

(b) Single frequency - pulse modulated.

(c) Four frequencies.

In each of these approaches it is assumed that the array has memory and remains in the last state commanded. To eliminate loss of the array by a single failure, the memory is cleared by power-off power on, to return the array to the primary mode of operation.

In the single frequency-time modulated approach, the nature of the command transmitted depends upon the time duration of the command tone. For example, a command that was on for 32 frame times (approximately 11 ms) would step counters in both clock units and at the station from the present state to the next state. Approximately 0.2 second would be required to step the array through all sixteen states. The status of the array is transmitted to the surface in each frame. Stepping along to the desired state could, therefore, be an automatic or closed loop operation. By differentiating, stretching and shaping a push-button closure to an 11 ms gate the same arrangement could be operated in a manual, jogging mode. This scheme presumes the existence of either main or backup clock at both clock units at all times and is, therefore, a departure from the existing design.

The single-frequency-pulse modulated approach does not depend upon active clocks in the array and is, therefore, more flexible and more compatible with existing design. In this approach each pulse of command tone on the command line steps a counter comprised of four asynchronous latches or R-S flip-flops to the next 16 states. Each pulse may be tens or hundreds of milliseconds

in duration to permit adequate filtering. Two Schmitt triggers detect levels on the rising and falling pulse to reliably generate the set and reset pulses necessary to clock the latches. The Schmitt trigger scaling is derived from the prime power level. The latch which commands main or backup clock acts immediately. The contents of the other three latches are loaded into a command register at the next frame sync time. The state which follows each calibration mode is used to reset the pseudo-random noise generators to all ONES. This can be done if the least significant bit of the four asynchronous latches is the CAL ON-LISTEN bit.

4.4 FREQUENCY COMMAND

The third station-clock link approach consists of generating one, two, three or four tones in the station and detecting these frequencies in the clock/transmitter units. Presence of energy in each of these bands sets a latch which commands the array to the appropriate mode. Narrow band tone decoders similar to Signetics 567 could be implemented using CMOS to reduce power consumption. More simply bandpass filters could be implemented. Assuming each pole-pair arising in an active filter such as that shown in Figure VII-3, assuming 1 percent component tolerances, the worst case gain, bandwidth and center frequency solutions are shown for single stage filters with a design Q of 10.

Assume that each center frequency is $\sqrt{2}$ times the next lower frequency. The worst problem in choosing a threshold for W_o would be for the filter at W_o to have low gain, low Q and high center frequency while the filter at $\sqrt{2}\ W_o$ has high gain, high Q and low center frequency. With W_o normalized to unity the Laplace transforms of these two worst case filters is as follows:

AD-A079 355 BENDIX CORP NORTH HOLLYWOOD CALIF ELECTRODYNAMICS DIV F/G 17/1
SEAGUARD DESIGN STUDY. REVISION A.(U)
OCT 75 N00140-76-C-6038
UNCLASSIFIED 8-4311-REV-A NL

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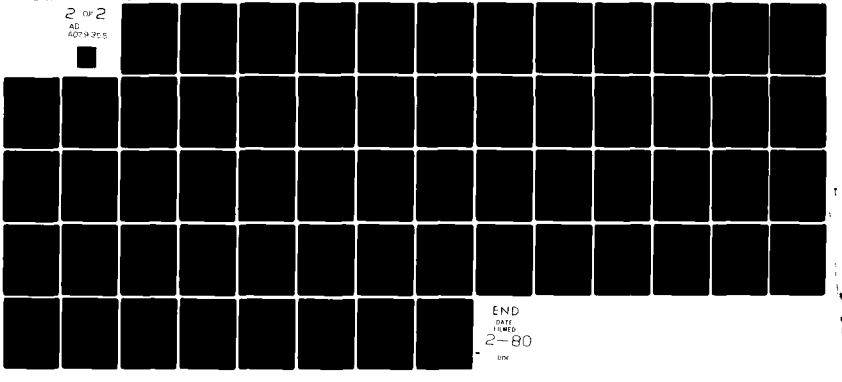


END
DATE FILMED
2-80
DDC

$$T_1(s) = \frac{.88315S}{S^2 + .15609S + 1.0408}$$

$$T_{\sqrt{2}}(S) = \frac{1.2490S}{S^2 + .06515S + 1.9216}$$

The steady-state frequency responses near W_o are shown in Figure VII-3 below.

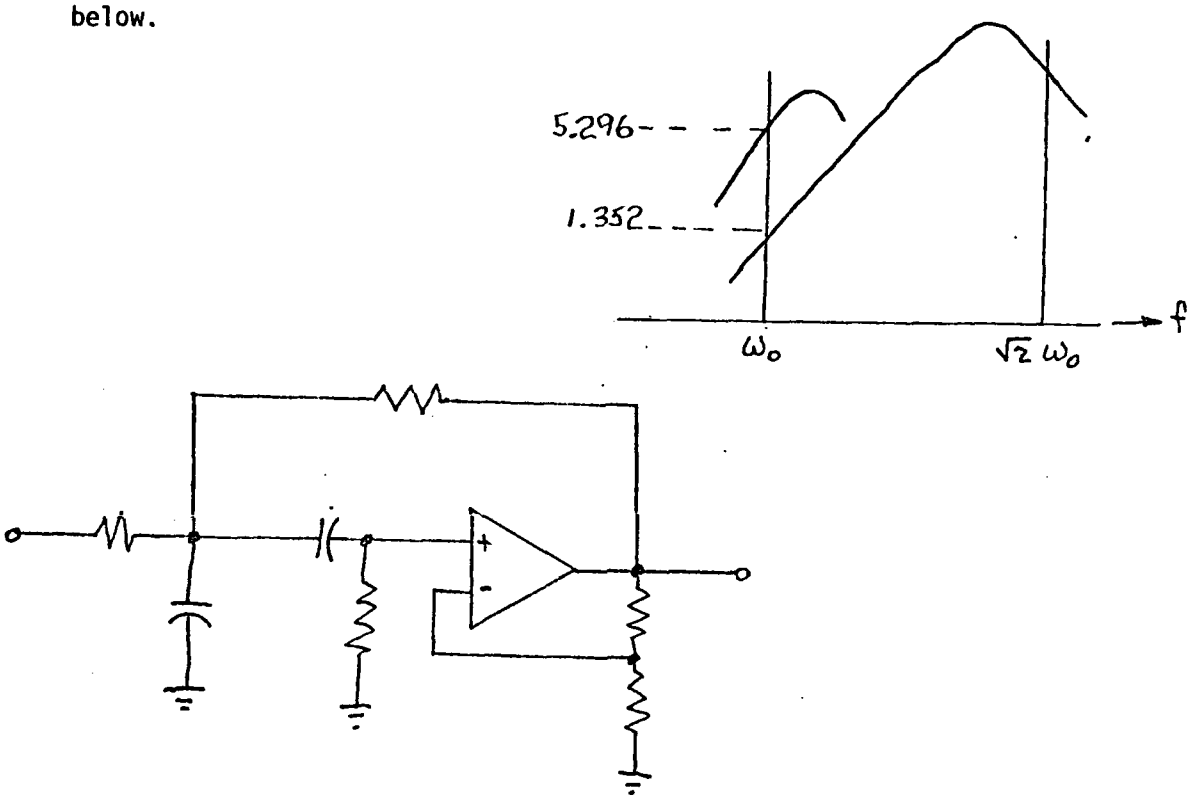


FIGURE VII-3.

The margin for the worst case combinations of this tentative design is 11.9 dB, which indicates that only single stage filters are necessary. The frequencies should be high in order to minimize capacitor size yet not high enough to interfere with data transmission or to result in excessive attenuation in the twisted pair. Choosing 20 kHz as the highest frequency, the command tones would be 7, 10, 14 and 20 kHz.

The existing tone detector occupies an area approximately 250 x 250 mils. The 1020 Hz Butterworth poles-pairs in the preamplifier with 1 percent components occupies area 300 x 250 mils. Each of the new tone detectors would probably be about this size and each would require one operational amplifier at 0.4 ma each (LM212). The larger power requirement is at the ACID repeater, with command level depending upon noise in the array and attenuation in the twisted pair. The repeater would require approximately 300 mw for reliable command transmission.

Four approaches are considered for the clock-transmitter link. These are identified by the lines over which the commands are transmitted.

(a) Clock Line Command.

(b) Data Line Command.

(c) Twisted Pair Command.

(d) Power Line Command.

Use of the main clock or backup clock should have no effect on transmitters. Listening to self-noise with low gain can be omitted. At present it appears that calibrating the system with the capacitor switched in would be a waste of effort. There remain five transmitter states which are significant. Listening or calibrating, with high or low gain, hydrophone switched in, require four states, and switching in the capacitor to evaluate self-noise with high gain is the fifth transmitter state. Two clock options result in a total of ten array states.

The present design (TLA system) uses the clock line to carry the BITE command to the transmitters. This approach could be expanded. Three double amplitudes represent one state, four the second, and so forth, with seven amplitude pulses being required for the fifth state. Since the normal

operating modes are included in these five states, the mode can be stored in the transmitters until a new command is received, or until a power off-power on cycle re-initializes. Alternatively the system could remain in a test mode for a fixed period of time and then return to a listening mode. If this feature is used a sixth state should exist, self-noise low gain, so that the operator does not have to re-insert "low gain" via "CAL-LOW GAIN". Reset to an operating mode can be done automatically by the dry end, if desired, by means of a mechanically latched push-button for gain and clock, and momentary push-buttons for CAL and self-noise.

The second approach to the clock-transmitter link is to use the status bits on the data line to generate mode commands for storage in the transmitter. In this scheme, the signal on the data line is coupled via equalization networks to a pair of comparators. Bipolar thresholds are established proportional to the clock signal amplitude. Clock periods are counted from frame sync time. At "gain-status" time the comparator outputs are sampled and the decision stored in a flip-flop. At the time corresponding to the hydrophone status bit the decision is stored in a second flip-flop and similarly for the calibration status bit. The output of these three flip-flops control the mode of operation for each transmitter.

The third approach considered would make use of the twisted pair (command line, station-clock link). Coupling capacitors would be used to bring in three of the four frequencies (if present) to set up storage of commands. DC commands cannot be used because of varying ground potentials. Command frequencies must be low compared to data and clock frequencies, and the size of the coupling capacitors becomes prhibitive unless high impedance circuits are used. These factors, plus the necessity for two more header pins, make this

approach less attractive than the two previously mentioned.

A fourth approach might use the power lines. Each transmitter has an impedance of from 1000 to 2000 ohms if the voltage across the unit is more than 16 volts. It is conceivable that ripple currents could be introduced and detected as commands. However, chokes would probably be required in the power source lines to keep the command power within bounds. With transmitters operating at a 3kHz frame rate it is not impossible there might be command frequency components in the transmitter load current that are not completely filtered. At the low voltage end of the array the system may be perfectly operable with Q_1 of some transmitters in a string saturated, these transmitters dropping sixteen volts, with a reduced current through VR1. These possibilities make further consideration of the power line path unnecessary.

The paths available to channel the commands from the clocks to the transmitters reduce to two. The equalization required to use status receivers in each transmitter depends upon the position of the transmitter in the array. If we apply the constraint that clock (and sync-status code) may originate on either the left or right, in order to simplify spares, then it becomes clear that the best clock-transmitter link is an extension of the method used in the present design, i.e., a multiplicity of double-amplitude pulses at frame-sync time.

APPENDIX A

PRELIMINARY POWER DISTRIBUTION INVESTIGATIONS

1. Voltage distribution for the full array (Configuration VI in the system constraints) using buffers. There are six configurations to investigate. These are:

(1) Parallel signal connections.

(a) Parallel power connections

(b) Center-fed power connections.

(c) Series power connections.

(2) Series signal connections

(a) Parallel power connections

(b) Center-fed power connections

(c) Series power connections

These configurations are illustrated in Figures A1 through A6 on the following pages.

From Figure A1:

$$E_{C1} = E_A - 12r_R - 4.62\ r_A - i_B(20r_R)$$

$$E_{IN1} = E_A = 12r_R - 20i_B r_R$$

$$E_{C2} = E_A - 12r_R - 2.31r_A - 7.92r_F - i_B(20r_R + 13.2r_F)$$

$$E_{IN2} = E_A - 12r_R - 7.92r_F - i_B(20r_R + 13.2r_F)$$

$$E_{C3} = E_A - 12r_R - 2.31r_A - 11.88\ r_F - i_B(20r_R + 11.88r_F)$$

$$E_{IN3} = E_A - 12r_R - 11.88r_F - i_B(20r_R + 11.88r_F)$$

$$E_{C4} = E_A - 12r_R - 4.62r_A - 15.84r_F - i_B(20r_R + 15.84r_F)$$

$$E_{IN4} = E_A - 12r_R - 15.84r_F - i_B(20r_R + 15.84r_F)$$

Letting the RISER equal one pair of AWG 12 wires (r_R = .794) and the array and feeder equal a pair of AWG 18 wires (r_A=r_F=3.1925), the following data

are derived. (See also Figure A7). Also let $i_B = 0.1$ amp.

$$E_{IN1} = E_A - 9.528 - 15.88\, i_B = E_A - 11.12$$

$$E_{C1} = E_A - 25.87$$

$$E_{IN2} = E_A - 40.61$$

$$E_{C2} = E_A - 47.99$$

$$E_{IN3} = E_A - 52.83$$

$$E_{C3} = E_A - 60.21$$

$$E_{IN4} = E_A - 66.75$$

$$E_{C4} = E_A - 81.50$$

From Figure A2 using the same criteria, the following data are derived (also see Figure A7):

$$E_{C2} = E_A - 110.73$$

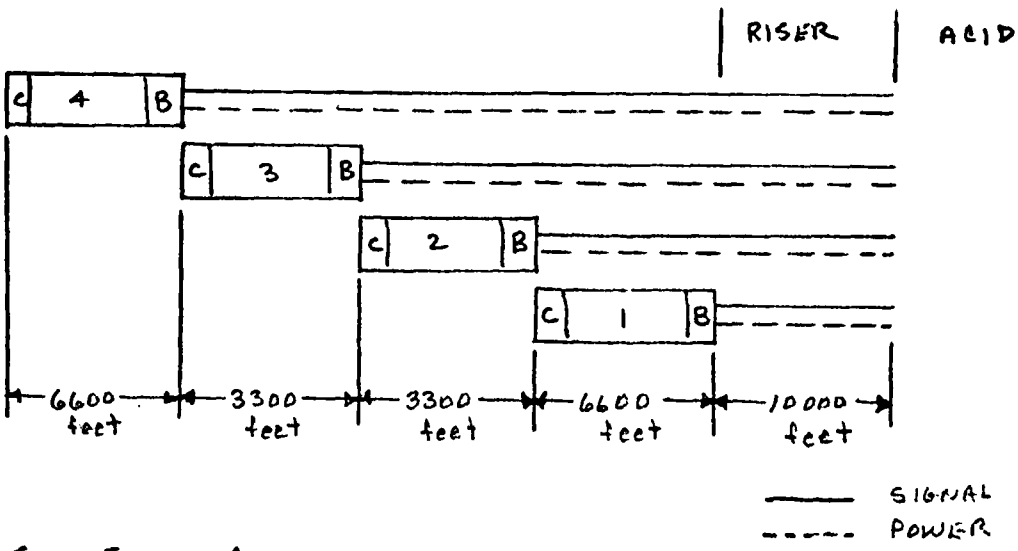
$$E_{IN2} = E_{C1} = E_A - 130.74$$

$$E_{IN1} = E_A - 145.50$$

$$E_{IN3} = E_A - 110.73$$

$$E_{IN4} = E_{C3} = E_A - 132.86$$

$$E_{C4} = E_A - 140.23$$



FOR EACH ARRAY:

$$E_C = E_A - (i_C + i_B + .05m) R_R - (i_C + \frac{.05m}{2}) R_A - (i_C + i_C + .05m) R_F$$

WHERE,

E_C = CLOCK STRING VOLTAGE = CLOCK + 4 TRANSMITTERS IN SERIES

E_A = VOLTAGE AT ACID

R_R = RISER RESISTANCE = $2 \cdot 10 \cdot r_R$

R_A = ARRAY RESISTANCE = $2 \cdot L \cdot r_A$

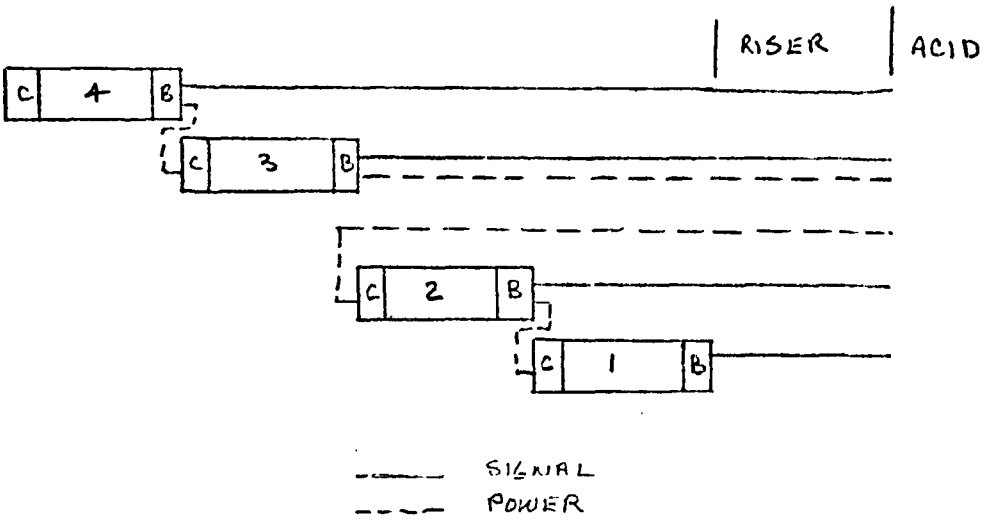
R_F = RISER TO ARRAY RESISTANCE = $2 \cdot L' \cdot r_F$

m = NUMBER OF TRANSMITTER STRINGS = 10 PER ARRAY

i_B = BUFFER CURRENT

i_C = CLOCK CURRENT = 0.1 amp

FIGURE A1



FOR DIMENSIONS SEE FIGURE A1

FIGURE A2

From Figure A3 using the same criteria, the following data are derived (also see Figure A7):

$$E_{IN1} = E_A - 159.59$$

$$E_{IN2} = E_{C1} = E_A - 262.83$$

$$E_{IN3} = E_{C2} = E_A - 300.67$$

$$E_{IN4} = E_{C3} = E_A - 322.80$$

$$E_{C4} = E_A - 337.55$$

From Figure A4 using the same wire sizes and i_B, the following data are derived (also see Figure A8):

$$E_{IN1} = E_{B1} = E_A - 11.91$$

$$E_{B2} = E_A - 13.43$$

$$E_{L1} = E_A - 15.09$$

$$E_{IN2} = E_A - 34.81$$

$$E_{B3} = E_A - 39.06$$

$$E_{L2} = E_A - 42.25$$

$$E_{IN3} = E_A - 47.46$$

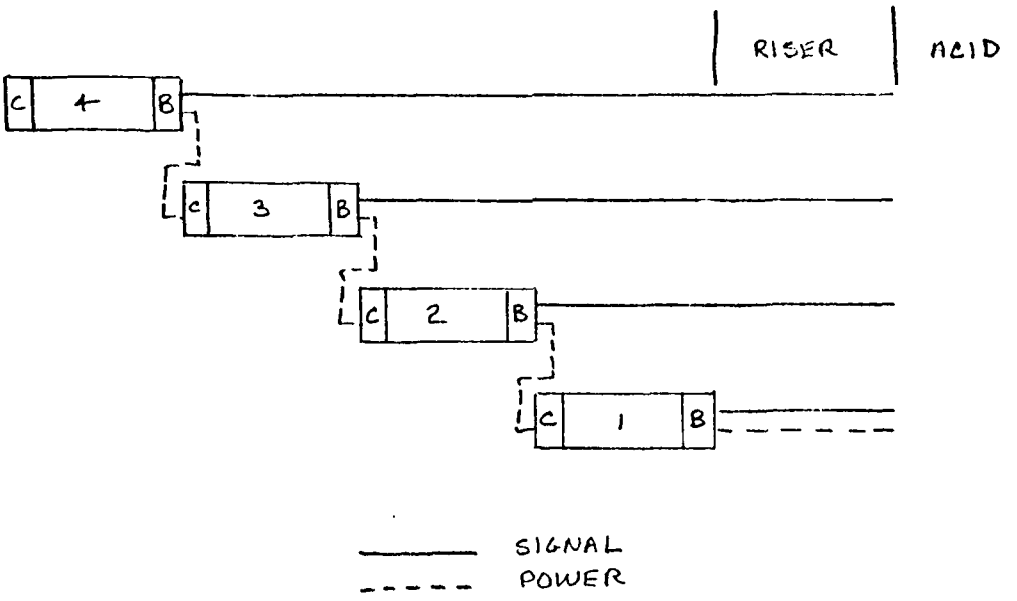
$$E_{B4} = E_A - 53.16$$

$$E_{L3} = E_A - 53.73$$

$$E_{IN4} = E_A - 63.21$$

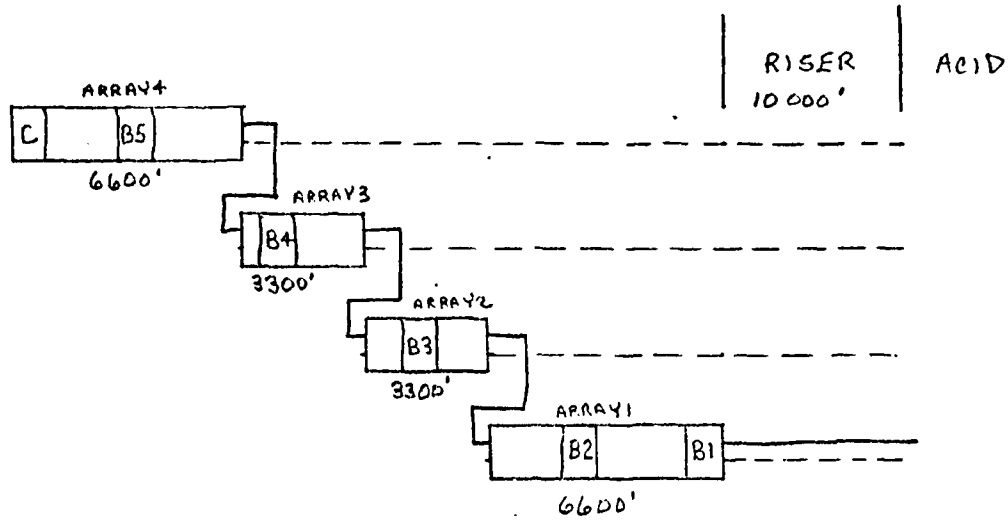
$$E_{B5} = E_A - 73.94$$

$$E_{L4} = E_{CLOCK} = E_A - 79.40$$



FOR DIMENSIONS SEE FIGURE A1

FIGURE A3



BUFFERS LOCATED EVERY 4000 FEET

FIGURE A4

From Figure A5 using the same criteria, the following data are derived (also see Figure A8):

$$E_{IN2} = E_A - 106.78$$

$$E_{B3} = E_A - 121.63$$

$$E_{IN1} = E_A - 130.56$$

$$E_{B2} = E_A - 141.34$$

$$E_{B1} = E_A - 148.37$$

$$E_{IN3} = E_A - 106.78$$

$$E_{B4} = E_A - 121.78$$

$$E_{IN4} = E_A - 128.10$$

$$E_{B5} = E_A - 138.93$$

$$E_{CLOCK} = E_A - 144.39$$

From Figure A6 using the same criteria, the following data are derived (see Figure A8):

$$E_{B1} = E_A - 42.88$$

$$E_{B2} = E_A - 104.82$$

$$E_{IN2} = E_A - 138.85$$

$$E_{B3} = E_A - 155.16$$

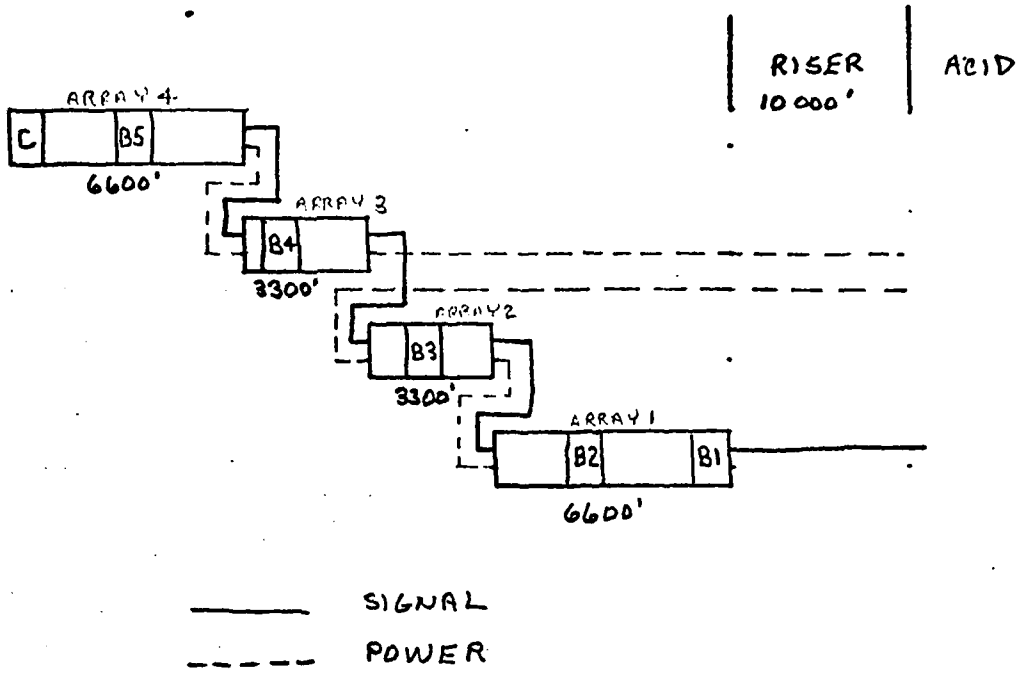
$$E_{IN3} = E_A - 173.15$$

$$E_{B4} = E_A - 188.91$$

$$E_{IN4} = E_A - 195.22$$

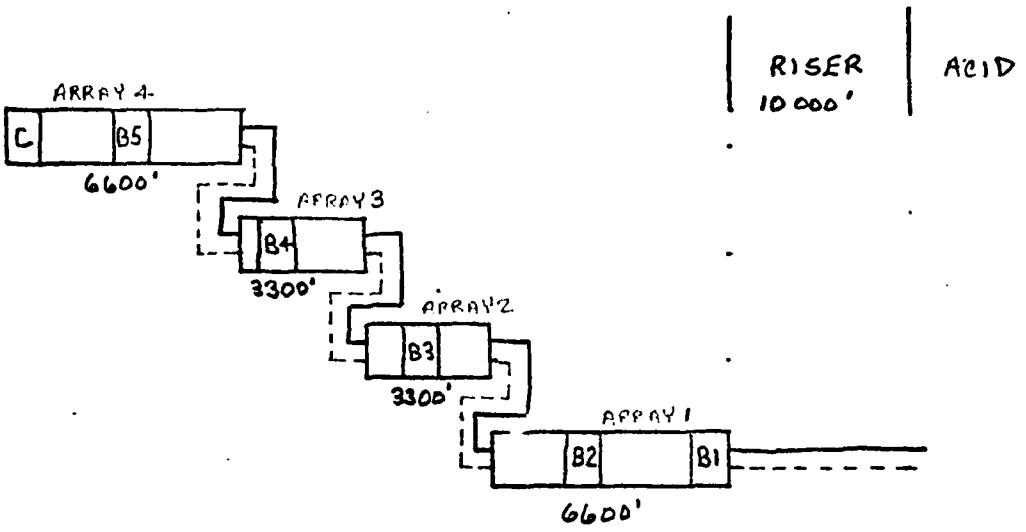
$$E_{B5} = E_A - 205.95$$

$$E_{CLOCK} = E_A - 211.41$$



BUFFERS LOCATED EVERY 4000 FEET

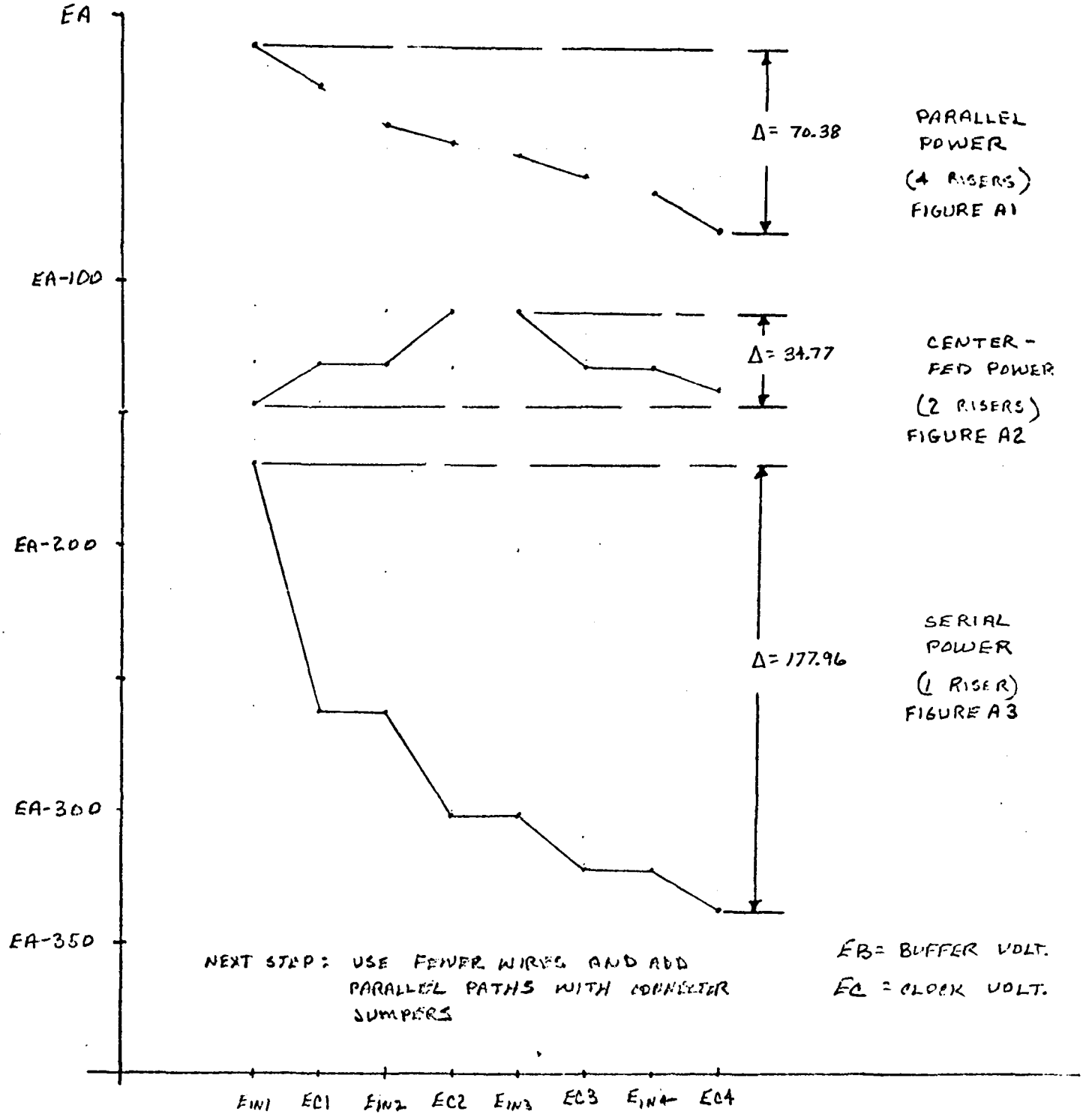
FIGURE A5



BUFFERS LOCATED EVERY 4000 FEET

FIGURE A6

PARALLEL SIGNAL CONNECTIONS



RISER WIRE = PAIR AWG 12 (+V), PAIR AWG 12 (RETURN) (see above

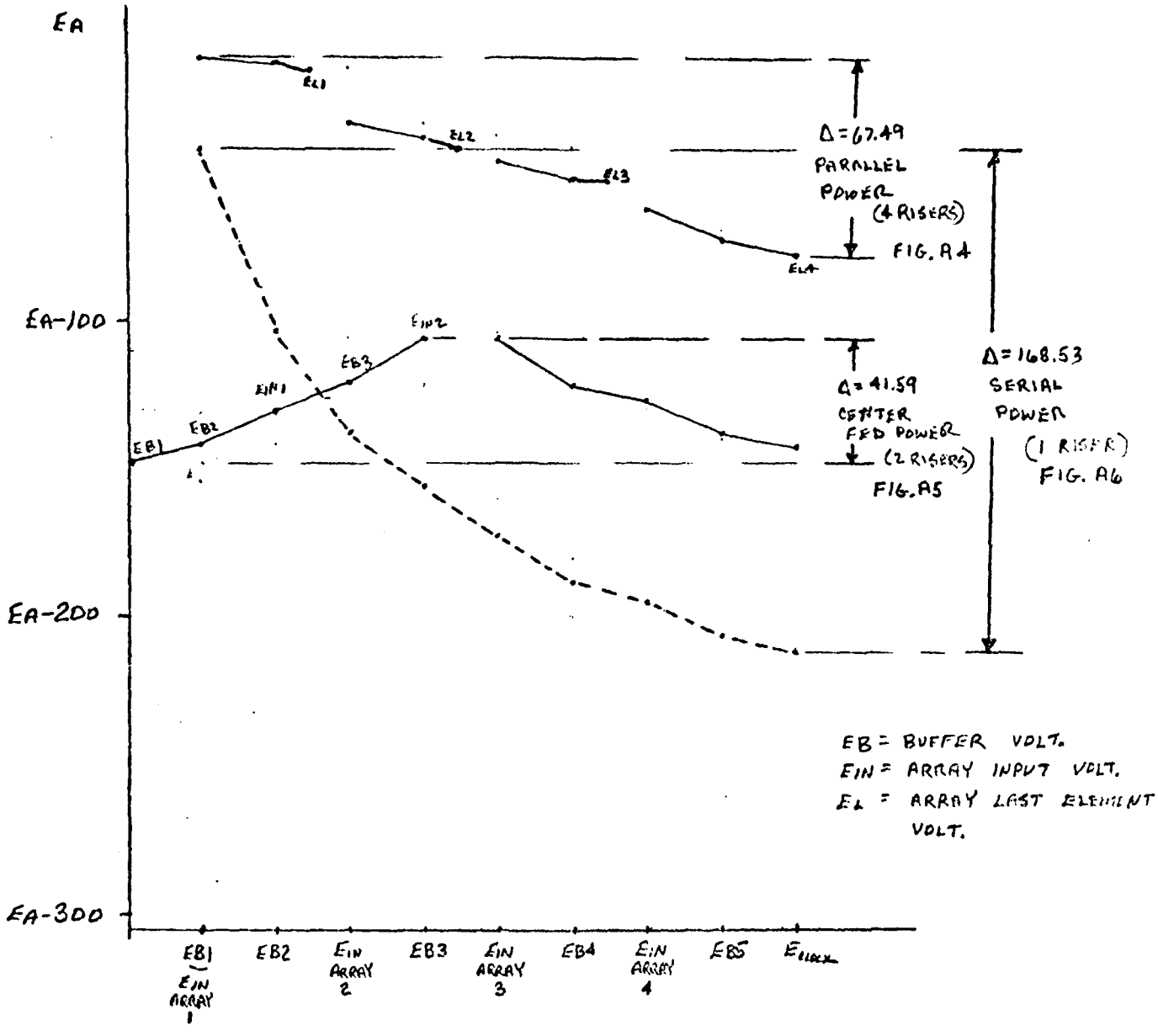
ARRAY WIRE = PAIR AWG 18 (+V), PAIR AWG 18 (RETURN)

BUFFER CURRENT = 100 ma, CLOCK CURRENT = 100 ma

TRANSMITTER CURRENT = 50 ma

Figure A7

SERIAL SIGNAL CONNECTIONS



RISER WIRE = PAIR AWG 12 (+V), PAIR AWG 12 (RETURN) (SEE ABOVE)

ARRAY WIRE = PAIR AWG 18 (+V), PAIR AWG 18 (RETURN)

BUFFER CURRENT = 100 ma
CLOCK CURRENT = 100 ma
TRANSMITTER CURRENT = 50 ma

NEXT STEP : USE FEWER WIRES AND ADD PARALLEL PATHS WITH CONNECTOR JUMPERS

Figure A8

The data shows that, for either type of signal distribution, the parallel or center-fed power distribution will work. That is, that the maximum difference in element voltage is less than

$$6(E_{max}) - 6(E_{min})$$

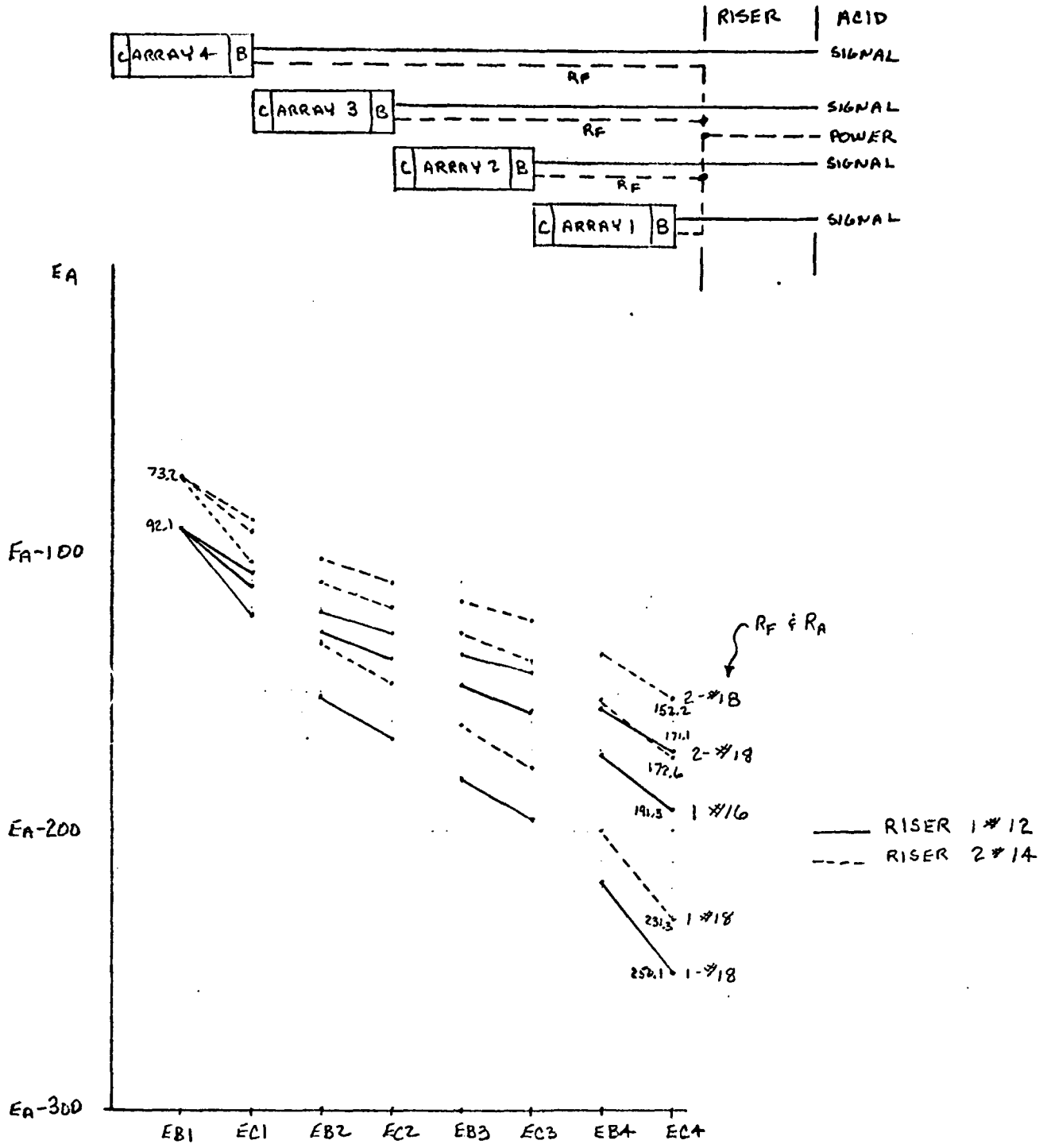
which for TLA elements is

$$6(30) - 6(16) = 92 \text{ volts.}$$

Using a series power connection with either signal distribution results in such high voltage differences that an ACID voltage could not be chosen to cause all element voltages to fall within the allowed range.

2. The next step is to evaluate using only one riser instead of one riser for each feed point. Because of the negative results in the previous section regarding a serial power system, those two cases are not considered.

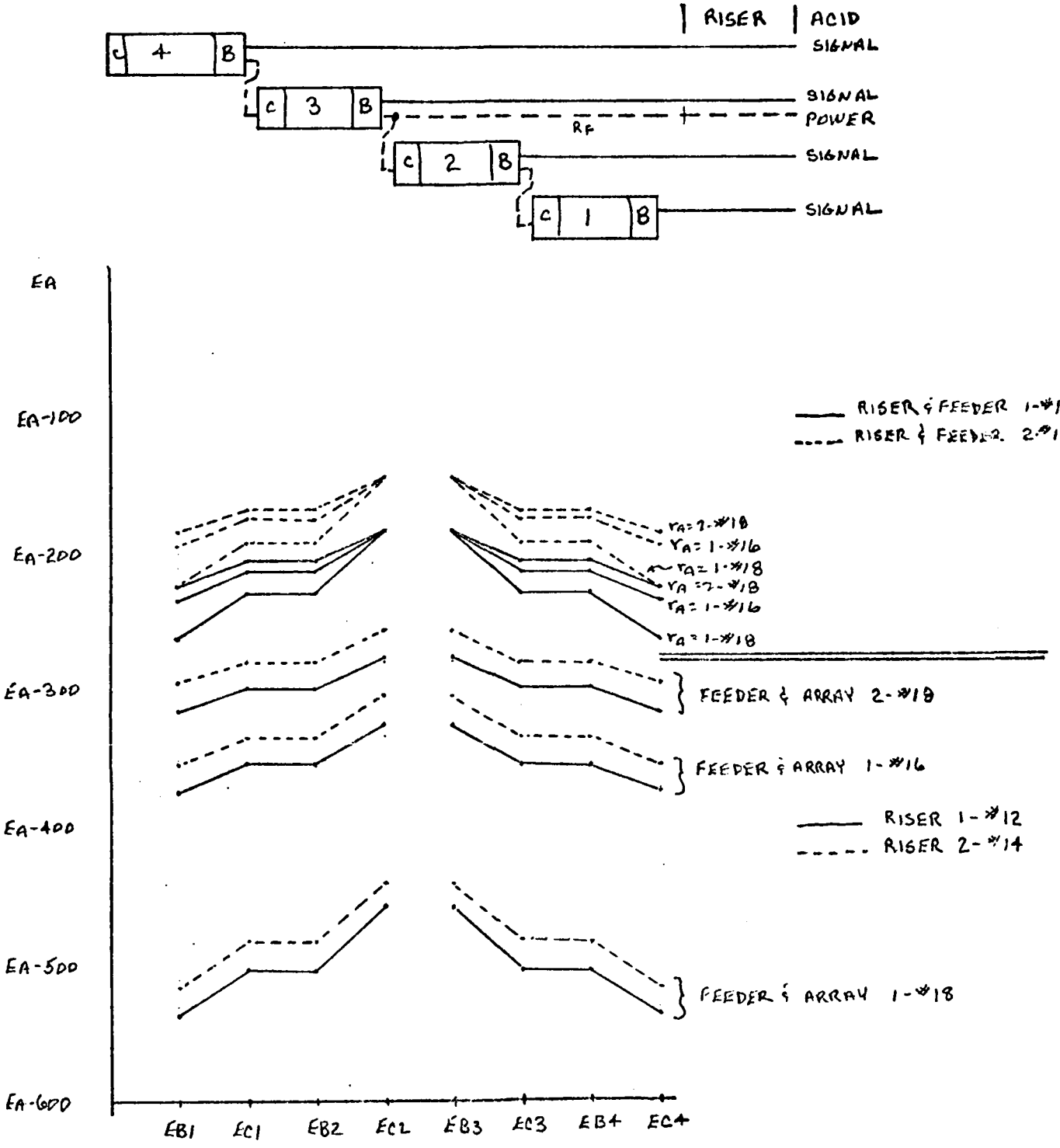
Lumped constant line resistances are used as in the previous section. Similar equations lead to the results plotted in Figures A9 through A12.



PARALLEL SIGNAL & POWER CONNECTIONS

NEXT STEP: USE AWG 18 WIRES IN ARRAY AND ADD PARALLEL WIRES WITH CONNECTOR JUMPERS

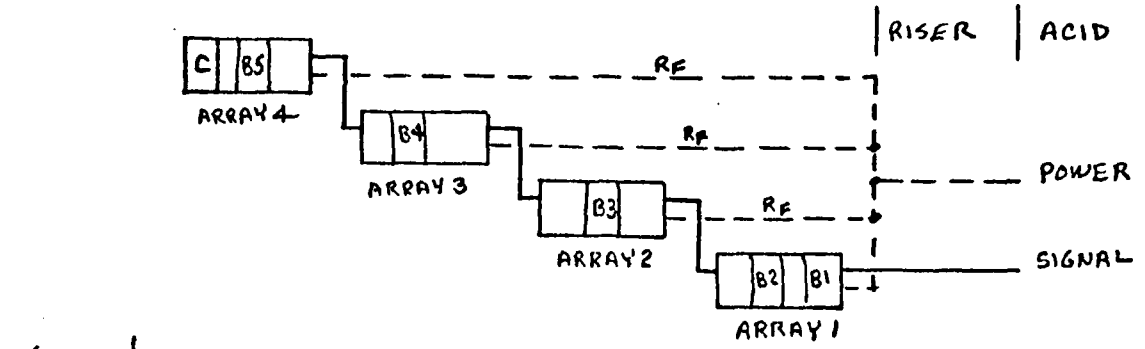
FIGURE A9

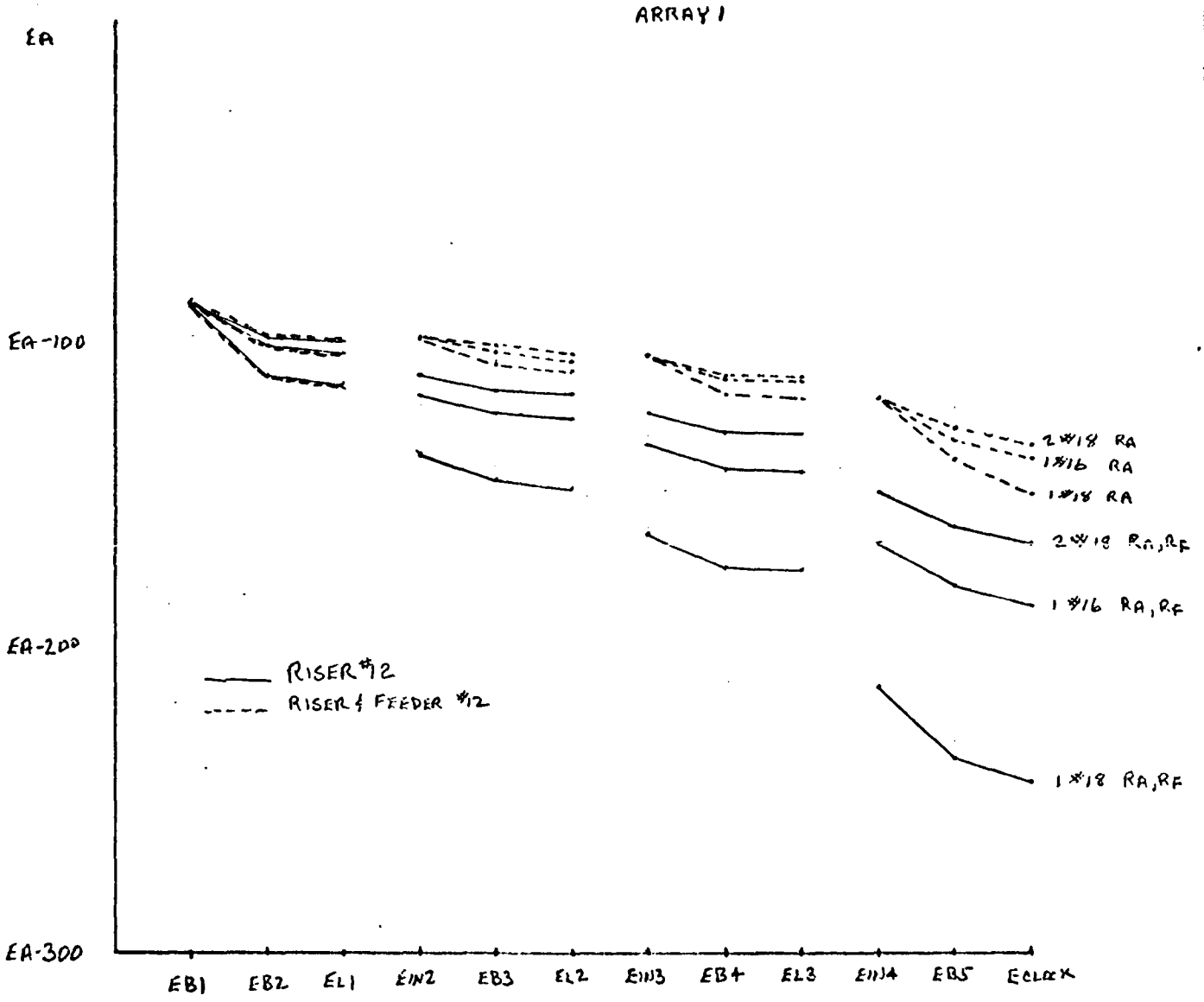


PARALLEL SIGNAL & CENTER FED POWER

NEXT STEP: USE AWG 18 WIRES AND ADD PARALLEL PATHS WITH CONNECTOR JUMPERS

FIGURE A10

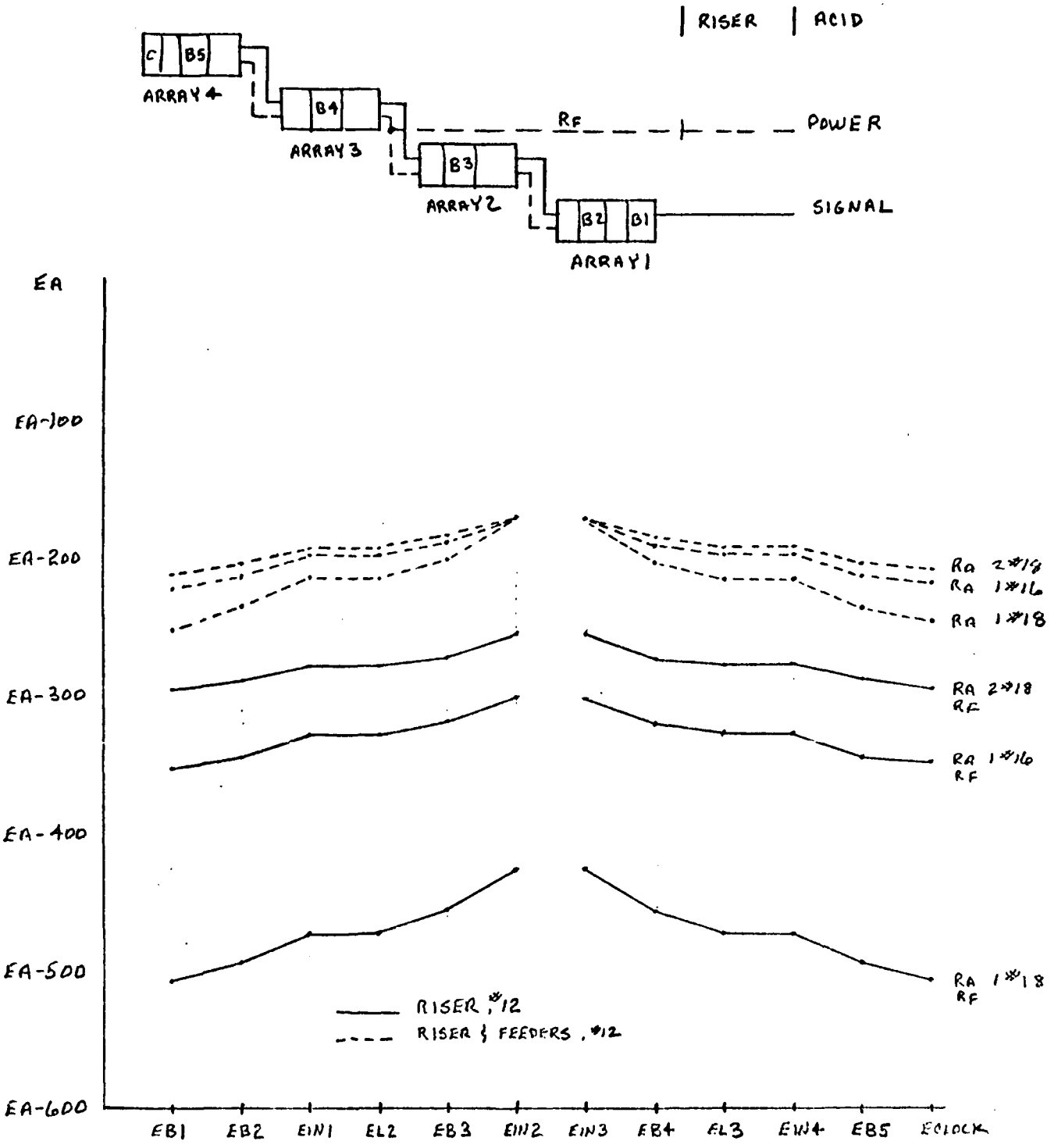




SERIAL SIGNAL - PARALLEL POWER CONNECTIONS

NEXT STEP: USE AWG 18 WIRES AND ADD PARALLEL PATHS WITH CONNECTOR JUMPERS.

FIGURE A11

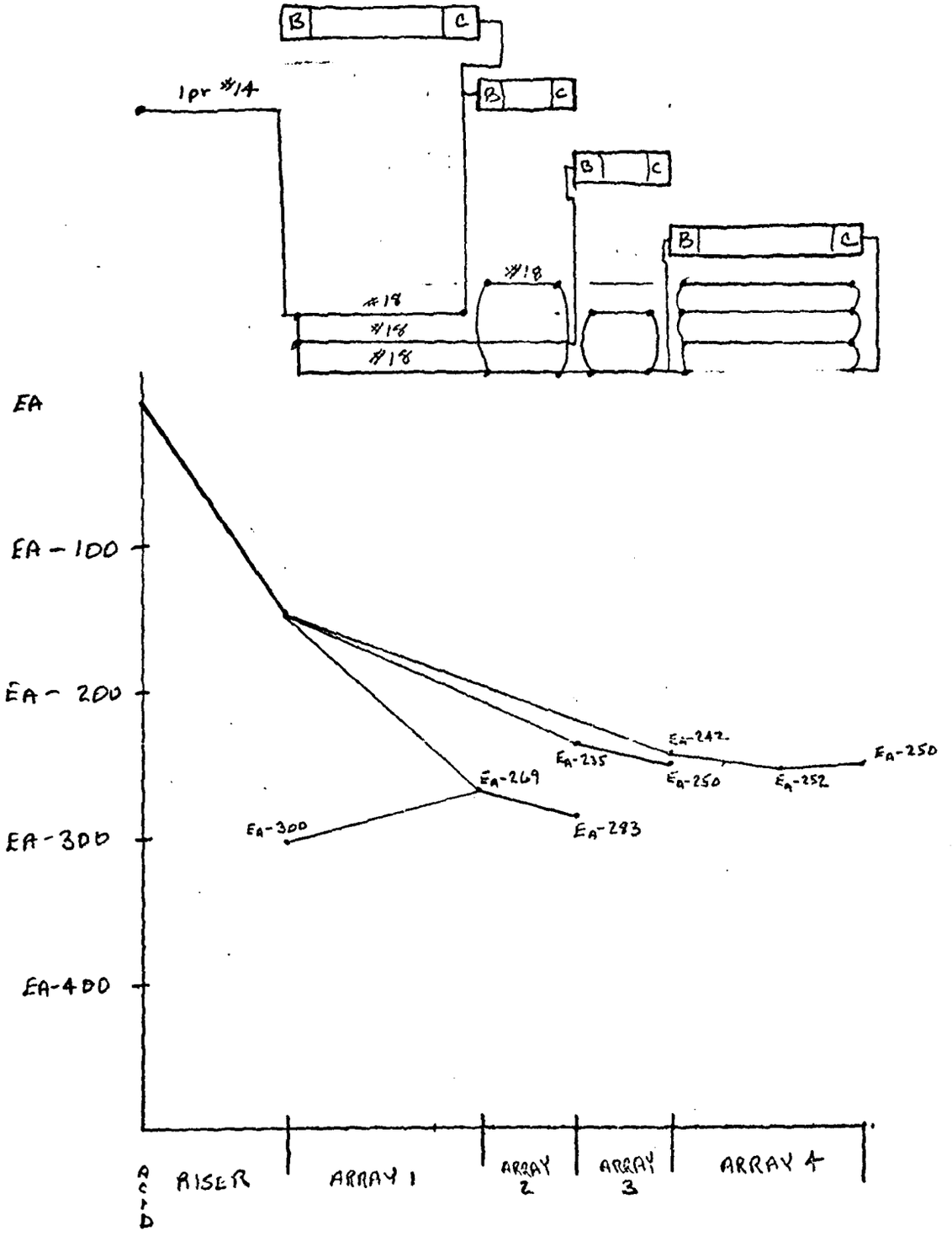


SERIAL SIGNAL - CENTER FED POWER

NEXT STEP: USE AWG-18 WIRES AND ADD PARALLEL PATHS WITH CONNECTOR JUMPERS

FIGURE A12.

3. The next step is to evaluate the use of AWG 18 wires through the array. It was decided to parallel conductors to feed the last section. One AWG 14 wire is used in the riser. The layout and voltage results are shown in Figure A13. The values shown for array 4 are derived reiteratively.



PARALLEL SIGNAL DISTRIBUTION

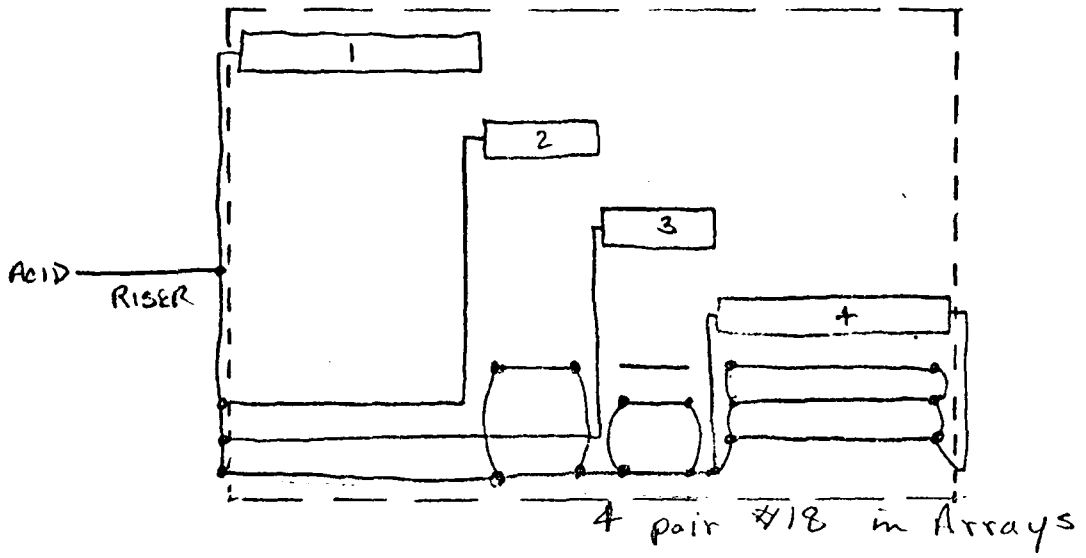
(BUFFER POWER INCLUDED

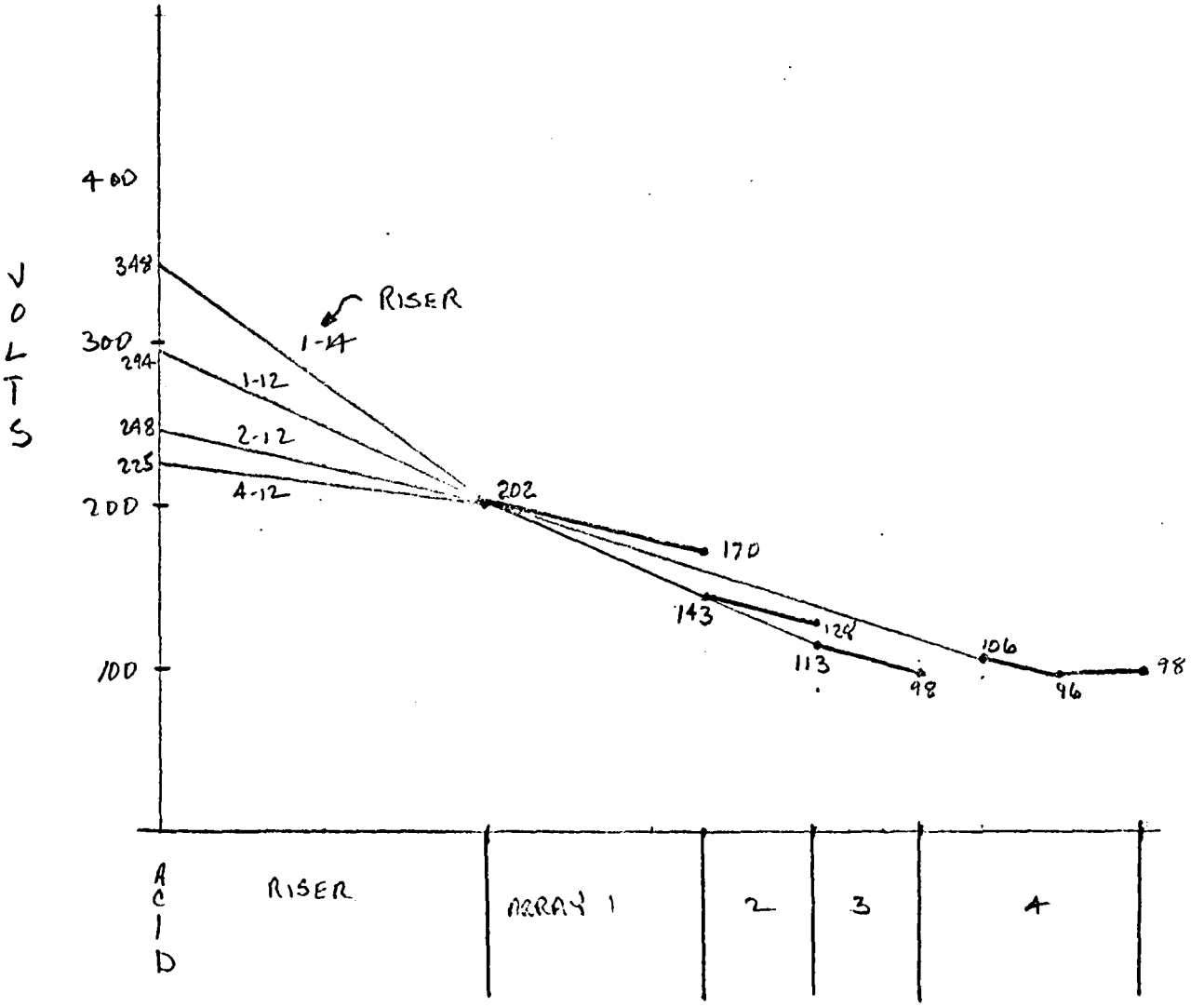
NEXT STEP = SEPARATE ARRAY 1 TO IT'S OWN RISER

FIGURE A13

4. The next step is to separate array 1 from array 2 and feed each one separately. With the minimum element voltage equal to 96 volts, a voltage of 202 volts is required at the array and of the riser. Four different riser wire sizes are investigated. This results in ACID voltages between 225 and 348 volts. The results of this investigation are shown in Figure A14.

(NOTE: Later data from TLA investigations indicates that 113 volts should be used for a minimum voltage.)

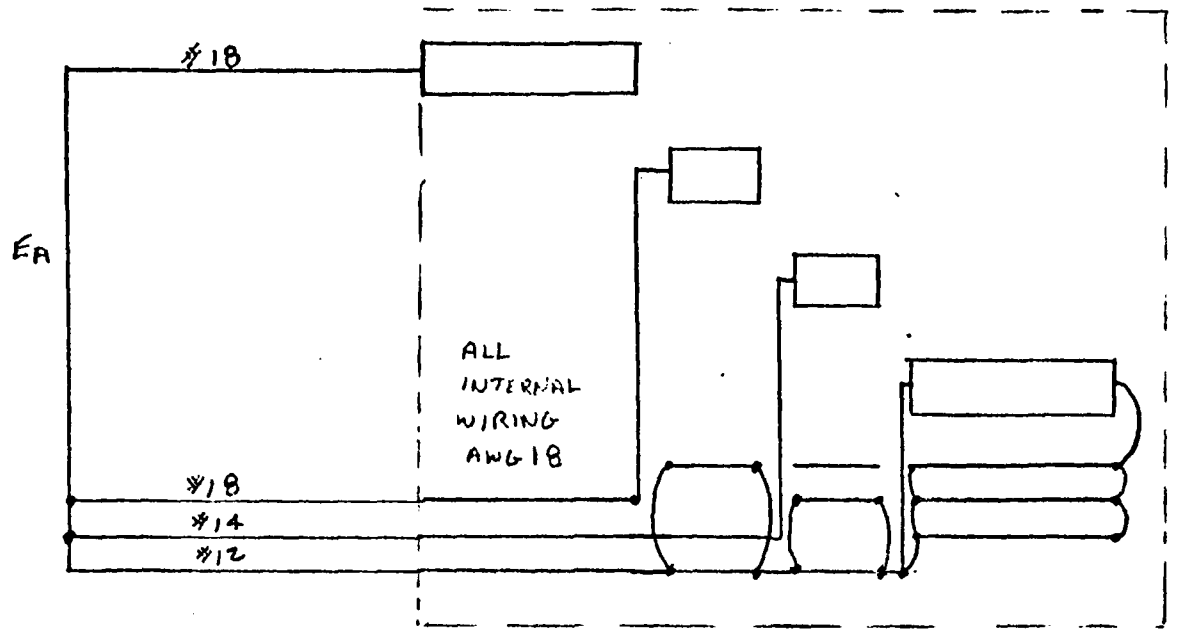


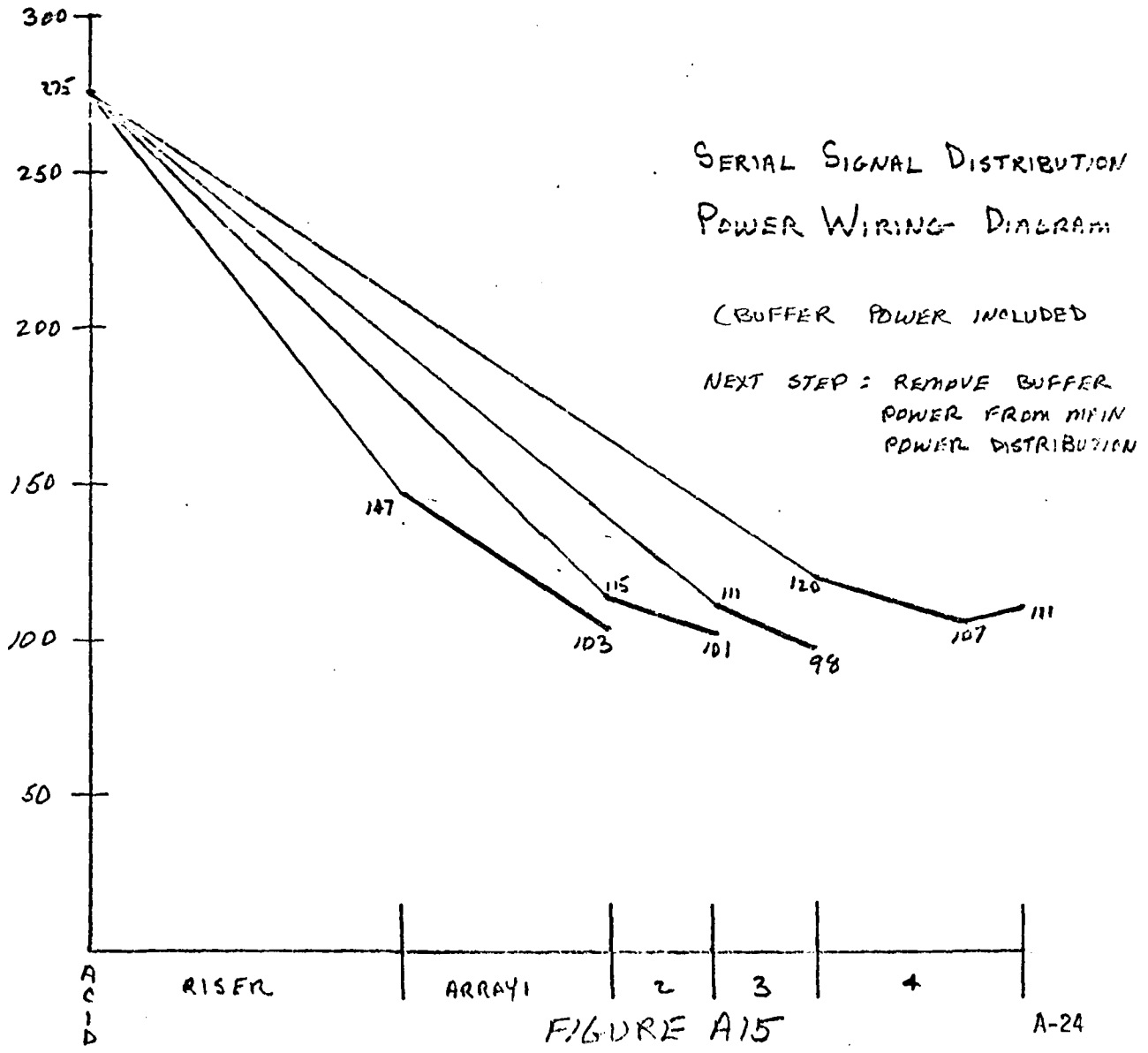


NEXT STEP : SEPARATE RISERS

FIGURE A14

5. The next step is to allow each array to be fed by a separate wire in the riser. The size of the riser wires could then be chosen to provide proper voltage drops for safe voltage limits on each array. The results of this investigation are shown in Figures A15 and A16 for the two different methods of signal distribution. The next step is to remove the buffer power from the main power distribution system. The results of this investigation are included in Section 2.1.4 of the main report.



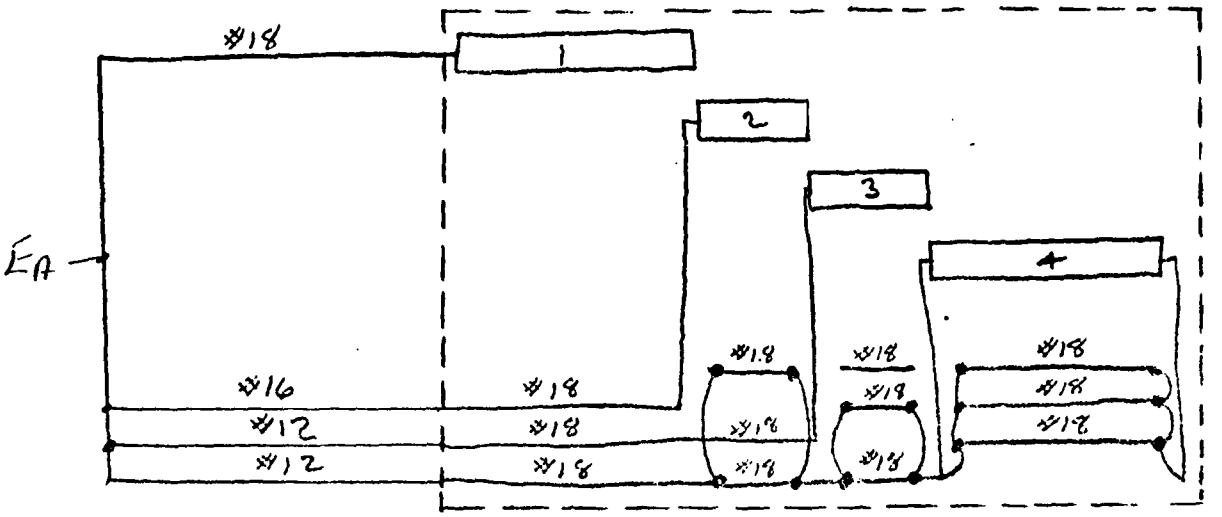


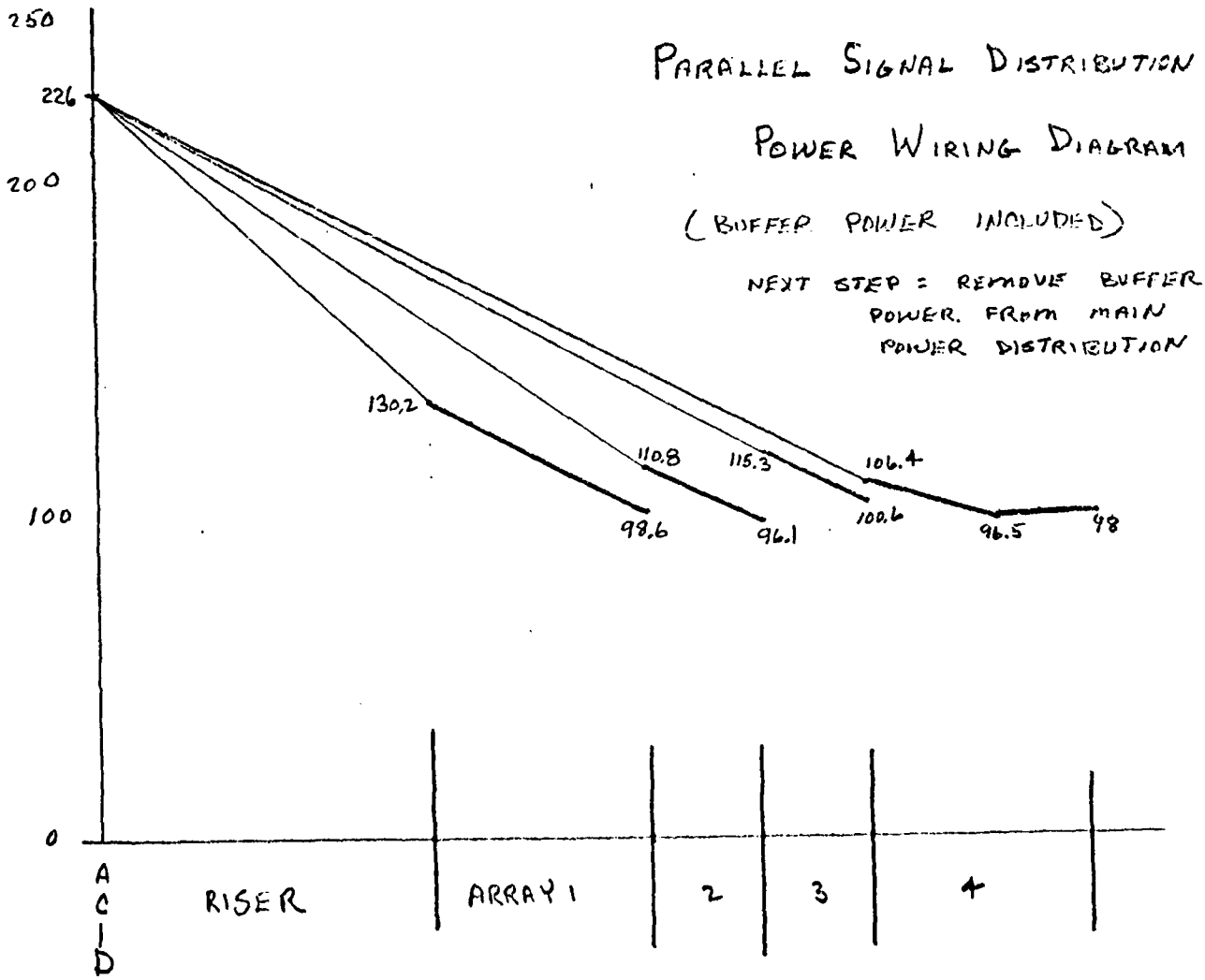
SERIAL SIGNAL DISTRIBUTION
POWER WIRING DIAGRAM

(BUFFER POWER INCLUDED

NEXT STEP: REMOVE BUFFER POWER FROM MAIN POWER DISTRIBUTION

FIGURE A15





PARALLEL SIGNAL DISTRIBUTION

POWER WIRING DIAGRAM

(BUFFER POWER INCLUDED)

NEXT STEP = REMOVE BUFFER POWER FROM MAIN POWER DISTRIBUTION

FIGURE A16

APPENDIX B

CONTINUOUS CABLE SYSTEM

Having received the request to investigate a system using a continuous cable from the ACID through the array and back to the anchor, the following system has been configured.

Parallel Signal Distribution

$$E_{C1} = E_A - .65\ R_{R1} - \frac{1}{2}(.55)R_{A1} - .1\ R_{A1}$$

But $r_R = r_A$ and

$$E_{C1} = E_A - .65(20)r_{R1} - \frac{1}{2}(.55)(13.2)r_{R1} - .1(13.2)r_{R1}$$

$$\simeq E_A - 17.95\ r_{R1}$$

$$E_{C2} = E_A - 22.23 r_{R2}$$

$$E_{C3} = E_A - 26.19\ r_{R3}$$

$$E_{C4} = E_A - 35.11\ r_{R4}$$

Let r_{RA} be AWG12 then, r_{R4} = 1.588Ω/1000 feet

E_{C4} = 113 volts (minimum)

then, E_A = 113 + 35.11 (1.588) = 168.8V

Let E_A = 170 volts

$$r_{R1} = \frac{170-113}{17.95} = 3.175 \text{ (maximum)}$$

use r_{R1} = AWG14 = 2.525 Ω/1000 feet

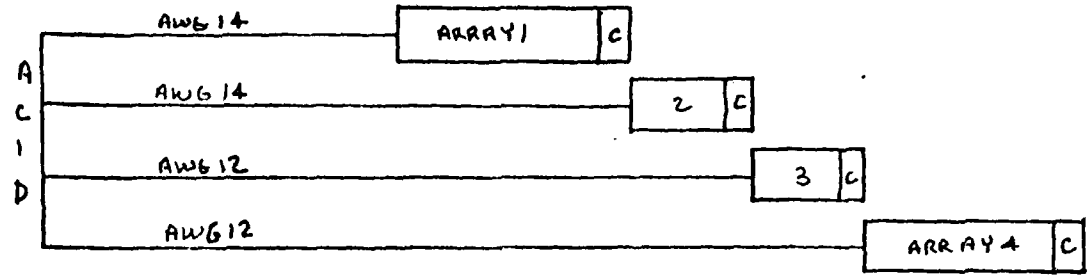
$$r_{R2} = \frac{170-113}{22.23} = 2.564 \text{ (maximum)}$$

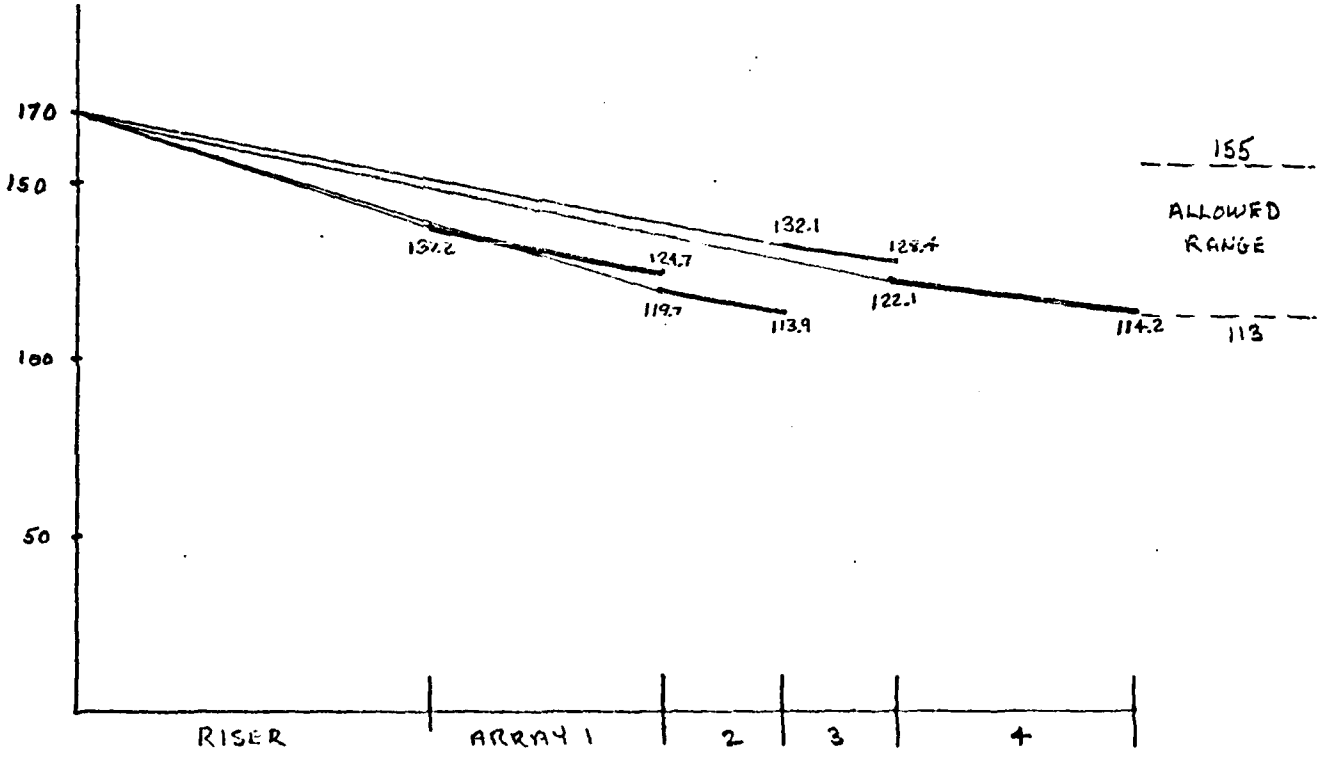
use r_{R2} = AWG14 = 2.525 Ω/1000 feet

$$r_{R3} = \frac{170-113}{26.19} = 2.176 \text{ (maximum)}$$

use r_{R3} = AWG12 = 1.588 Ω/1000 feet

Using these riser/array combinations the data was obtained to plot Figure B-1.





PARALLEL SIGNAL DISTRIBUTION

FIGURE B1

Serial Signal Distribution

$$E_{IN1} = E_A - .55\ R_{R1} = E_A - 11\ r_{R1}$$

$$E_{LOW1} = E_A - .55\ R_{R1} - \tfrac{1}{2}(.55)R_{A1}$$

since $r_A = r_R$

$$E_{LOW1} = E_A - 14.63\ r_{R1}$$

$$E_{IN2} = E_A - 16.6\ r_{R2}$$

$$E_{LOW2} = E_A - 18.25\ r_{R2}$$

$$E_{IN3} = E_A - 19.9\ r_{R3}$$

$$E_{LOW3} = E_A - 21.55\ r_{R3}$$

$$E_{IN4} = E_A - 30.16\ r_{R4}$$

$$E_{LOW4} = E_A - 35.11\ r_{R4}$$

Let r_{R4} be AWG12, r_{RA} = 1.588 Ω/1000 feet

E_{LOW4} = 113 volts (minimum)

then,

$E_A = 113 + 35.11(1.588) = 168.8$

Let E_A = 170 volts

$r_{R1} = \frac{170-113}{14.63} = 3.896$ (maximum)

use AWG14, r_{R1} = 2.525 Ω/1000 feet

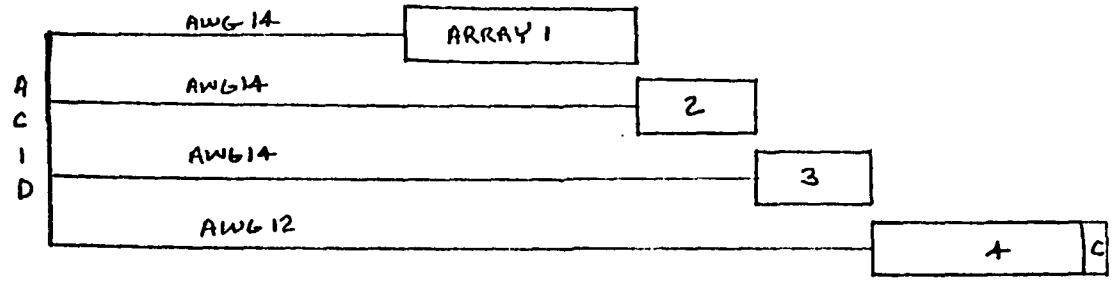
$r_{R2} = \frac{170-113}{18.25} = 3.123$ (maximum)

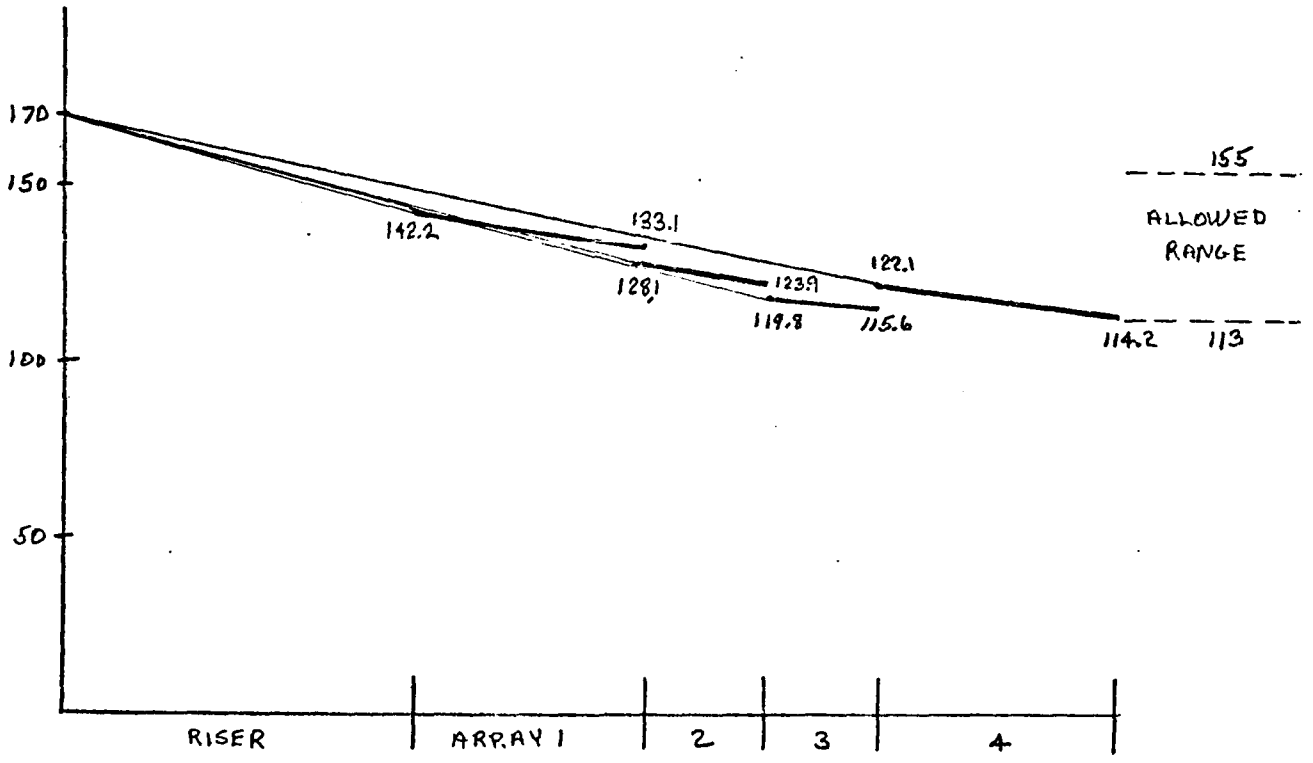
use AWG14, r_{R2} = 2.525 Ω/1000 feet

$r_{R3} = \frac{170-113}{21.55} = 2.645$ (maximum)

use AWG14, r_{R3} = 2.525 Ω/1000 feet

Using the above values, the data was calculated to plot Figure B-2.





SERIAL SIGNAL DISTRIBUTION

FIGURE B2

Power Cable Weight

Using Teflon insulated wire per MIL-W-16878D, Type E, 600 volts, the following power cable weights were obtained.

Parallel Signal Distribution System

Riser = 10(15.19 + 15.19 + 22.41 + 22.41)(2) = 1504 pounds.

Array 1 = 6.6(15.19 + 15.19 + 22.41 + 22.41)(2) = 992.64 pounds.

Array 2 = 3.3(75.2)(2) = 496.32 pounds.

Array 3 = 3.3(75.2)(2) - 496.32 pounds.

Array 4 = 6.6(75.2)(2) = 992.64 pounds.

Anchor = 10(75.2)(2) = 1504 pounds.

TOTAL = 5986 pounds.

Serial Signal Distribution System

Riser = 10(15.19 = 15.19 = 15.19 = 22.41)(2)

= 10(67.98)(2)

= 1359.6 pounds

Array 1 = 6.6(67.98)(2)

= 897.3 pounds

Array 2 = 3.3 (67.98)(2)

= 448.7 pounds

Array 3 = 3.3(67.98)(2)

= 448.7 pounds

Array 4 = 6.6(67.98)(2)

= 897.3 pounds

Anchor = 10(67.98)(2)

= 1359.6

Total = 5411 pounds

Power Distribution

Using the same format as used in Section 2.1.3 of the main report, the power distribution is as shown in Tables B-1 and B-2. (Also see Figure B-3).

TABLE B-1

PARALLEL SIGNAL DISTRIBUTION

Array	Riser	Through Wires	Array Wire	Trans-mitter	Clock
1	21.3	28.4	8.1	72.0	12.5
2	18.2	8.2	3.5	58.4	11.4
3	11.4	4.4	2.2	65.1	12.8
4	13.4	-0-	5.1	65.0	11.4

TABLE B-2

SERIAL SIGNAL DISTRIBUTION

Array	Riser	Through Wires	Array Wire	Trans-mitter	Clock
1	15.3	25.5	5.0	75.7	-0-
2	12.6	8.6	2.1	63.0	-0-
3	12.6	4.4	2.1	58.9	-0-
4	13.4	-0-	5.1	65.0	11.4

POWER DISTRIBUTION

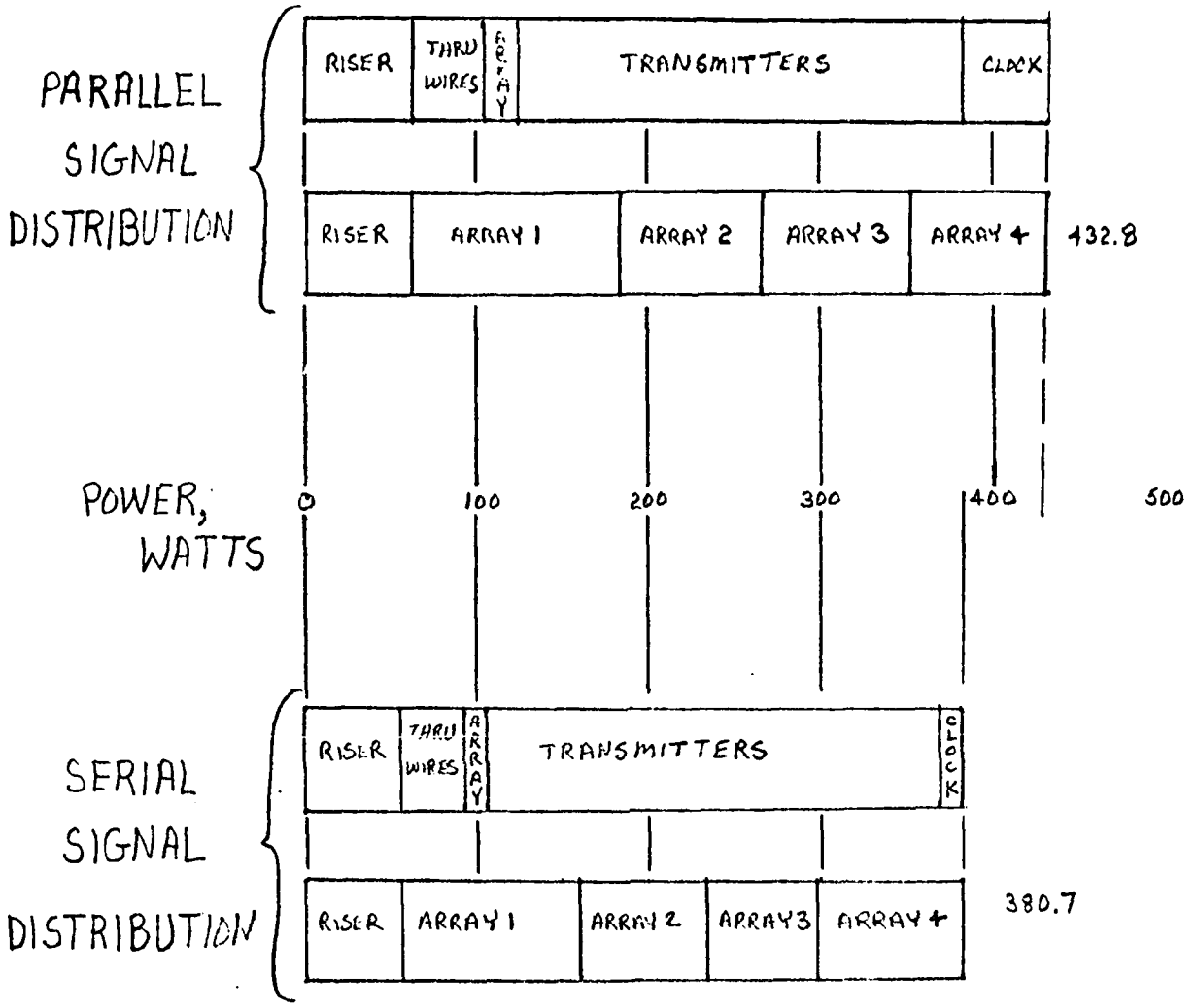


FIGURE B3

If one lets the efficiency of the system be related as follows:

$$\text{eff.} = \frac{\text{Power In Transmitters}}{\text{Power IN}} \times 100\%$$

Then Table B-3, below, describes the system efficiencies. These do not include losses in the ACID-to-ship cable.

	Efficiency, %	
	Parallel Signal Dist.	Serial Signal Dist.
Array 1	50.1	62.3
Array 2	58.6	73.0
Array 3	67.9	75.5
Array 4	68.5	68.5
System	60.2	69.0

The following investigation is into the use of a continuous cable but allows for the paralleling of conductors in the array. All transmitters will be connected to the smallest size wire. Only the serial signal distribution case is investigated.

Let r_1 = the resistance of the wire feeding array 1 and internally feeding each transmitter string.

r_2 = the resistance of the wire feeding array 2.

r_3 = the resistance of the wire feeding array 3.

r_4 = the resistance of the wire feeding array 4.

Using the array lengths and currents, the following relationships exists.

$$E_{IN1} = E_A - (.55)(20)r_1 = E_A - 11r_1$$

$$E_{L1} = E_A - (.55)(20)r_1 - (.5)(.55)(13.2)r_1 = E_A - 14.63r_1$$

$$E_{IN2} = E_A - 16.6r_2$$

$$E_{L2} = E_A - 16.6r_2 - 1.65r_1$$

$$E_{IN3} = E_A - 19.9r_3$$

$$E_{L3} = E_A - 19.9r_3 - 1.65r_1$$

Neglecting the wires paralleling array 4,

$$E_{IN4} = E_A - 21.58r_4 - 4.29\,\frac{r_1r_4}{r_1+r_4} - 4.29\,\frac{r_1r_2r_4}{r_2r_4+r_1r_4+r_1r_2}$$

$$E_{L4} = E_A - 21.58r_4 - 4.29\,\frac{r_1r_4}{r_1+r_4} - 4.29\,\frac{r_1r_2r_4}{r_2r_4+r_1r_4+r_1r_2} - 4.29r_1$$

Let array 1 wire be AWG 18.

then,

$$r_1 = 6.385$$

$$E_{IN1} = E_A - 70.235$$

$$E_{L1} = E_A - 93.41$$

$$E_{IN2} = E_A - 16.6r_2$$

$$E_{L2} = E_A - 16.6r_2 - 10.54$$

$$E_{IN3} = E_A - 19.9r_3$$

$$E_{L3} = E_A - 19.9r_3 - 10.54$$

If E_{IN} = 155 volts maximum

E_L = 113 volts minimum

E_A = 210 volts

then from the above equations,

$$r_2 = 3.313 \text{ minimum}$$

$$r_2 = 5.208 \text{ maximum}$$

$$r_3 = 2.764 \text{ minimum}$$

$$r_3 = 4.345 \text{ maximum}$$

For each of the above let the wire be AWG 16 with r = 4.016.

Substituting these resistances gives the following equations:

$$E_{IN1} = E_A - 70.2 = 139.8$$

$$E_{L1} = E_A - 93.4 = 116.6$$

$$E_{IN2} = E_A - 66.7 = 143.3$$

$$E_{L2} = E_A - 77.2 = 132.8$$

$$E_{IN3} = E_A - 79.9 = 130.1$$

$$E_{L3} = E_A - 90.5 = 119.5$$

Substituting the selected wire resistances and E_A into the equations for array 4 and letting E_{IN4} = 155 volts and E_{L4} = 113 volts, yields the following equations:

$$r_4^3 + 8.06\ r_4^2 - 0.56 r_4 - 40.12 = 0$$

$$r_4 = 2.023 \text{ minimum}$$

$$r_4^3 + 7.384\ r_4^2 - 6.55\ r_4 - 50.78 = 0$$

$$r_4 = 2.606 \text{ maximum}$$

Let array 4 wire be AWG 14 and r_4 = 2.525

then

$$E_{IN4} = 142.4$$

$$E_{L4} = 115.0$$

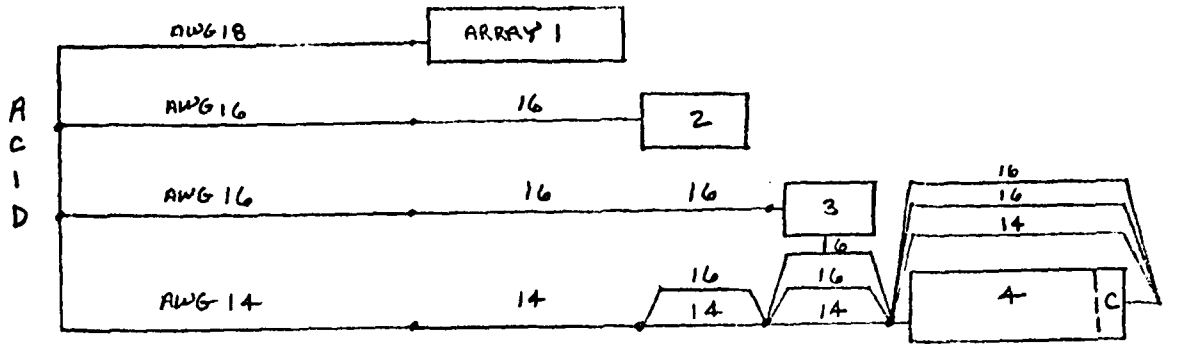
After adding the wires paralleling array 4 and solving the network for the current divisions, the following results were obtained:

$$E_{IN4} = 142.4$$

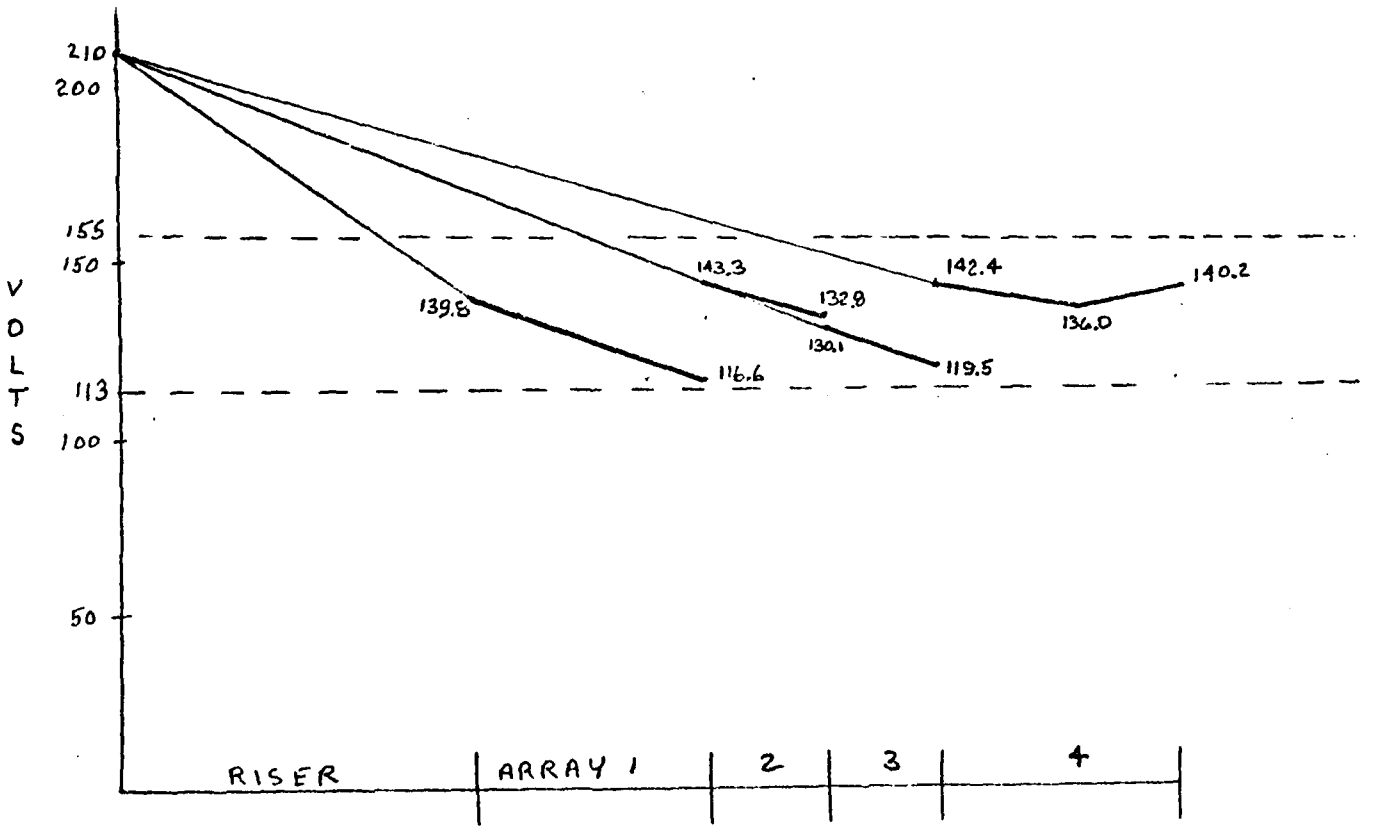
$$E_L = 136.0$$

$$E_{CLOCK} = 140.2$$

the results of the above evaluation are plotted in Figure B-4.



TRANSMITTERS ALWAYS CONNECTED TO AWG18 WIRES



SERIAL SIGNAL DISTRIBUTION

FIGURE B4

Power Cable Weight

Using Teflon insulated wire per MIL-W-16878D, Type E, 600 volts, the following power cable weights were obtained:

Riser = 865.2 pounds

Array 1 = 571.0 pounds

Array 2 = 285.5 pounds

Array 3 = 285.5 pounds

Array 4 = 571.0 pounds

Anchor = 865.2 pounds

TOTAL = 3443.4 pounds.

This is 64 percent of the previous approach.

Power Distribution

Using the techniques in the main report, the power distribution shown in Figure B-5 was derived.

Using the previous definition of efficiency the efficiencies are as follows:

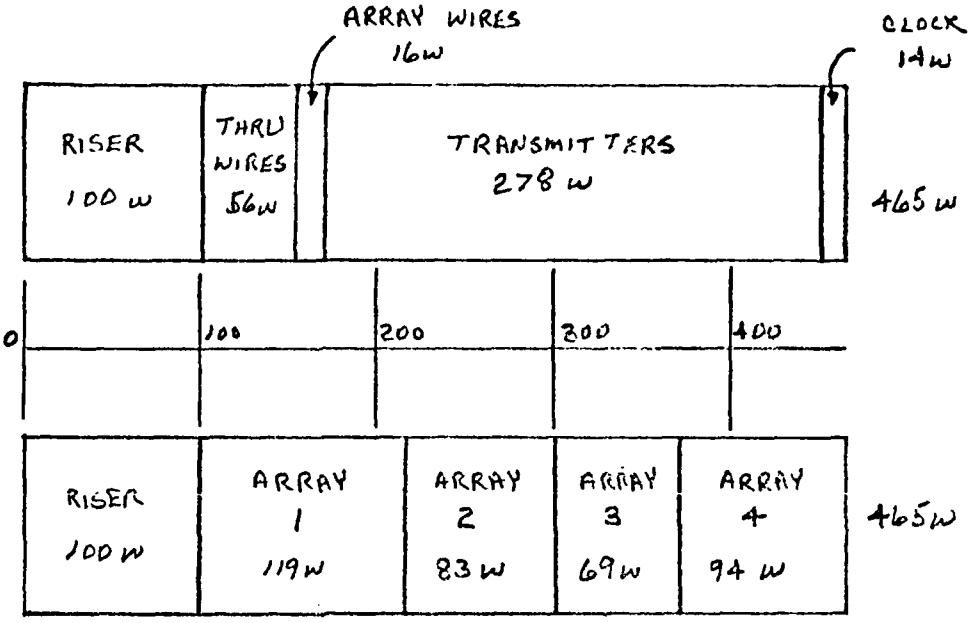
Array 1 - 45 percent

Array 2 - 67 percent

Array 3 - 70 percent

Array 4 - 66 percent

Total - 60 percent



POWER DISTRIBUTION

FIGURE B5

THE
BENDIX
CORPORATION

Electrodynamics
Division

North Hollywood
California

COAX CABLE

PRESSURE TEST

FINAL REPORT

Report No.
HRS-75-018

1.0 INTRODUCTION

The purpose of the test is to determine the electrical useability of RG58-B/U coax cable when repeatedly subjected to a pressure of 10,000 pounds per square inch. The test was run in accordance with Memo HRS-75-014, "Test Plan Coax Pressure Test". A one-thousand foot length of coax cable was tested.

2.0 TEST SET UP

The test set up is shown in Figure 1. The coax cable was taken from the spool and evenly spread over a four-foot frame in order to expose all of the cable to the same conditions. Extreme care was used in handling to prevent damage to the cable jacket.

The following test equipment was used:

A. For Attenuation:

HP606A Signal Generator

HP34750A Digital Readout

HP34703A Multimeter

B. For DC Resistance:

HP34750A Digital Readout

HP34703A Multimeter

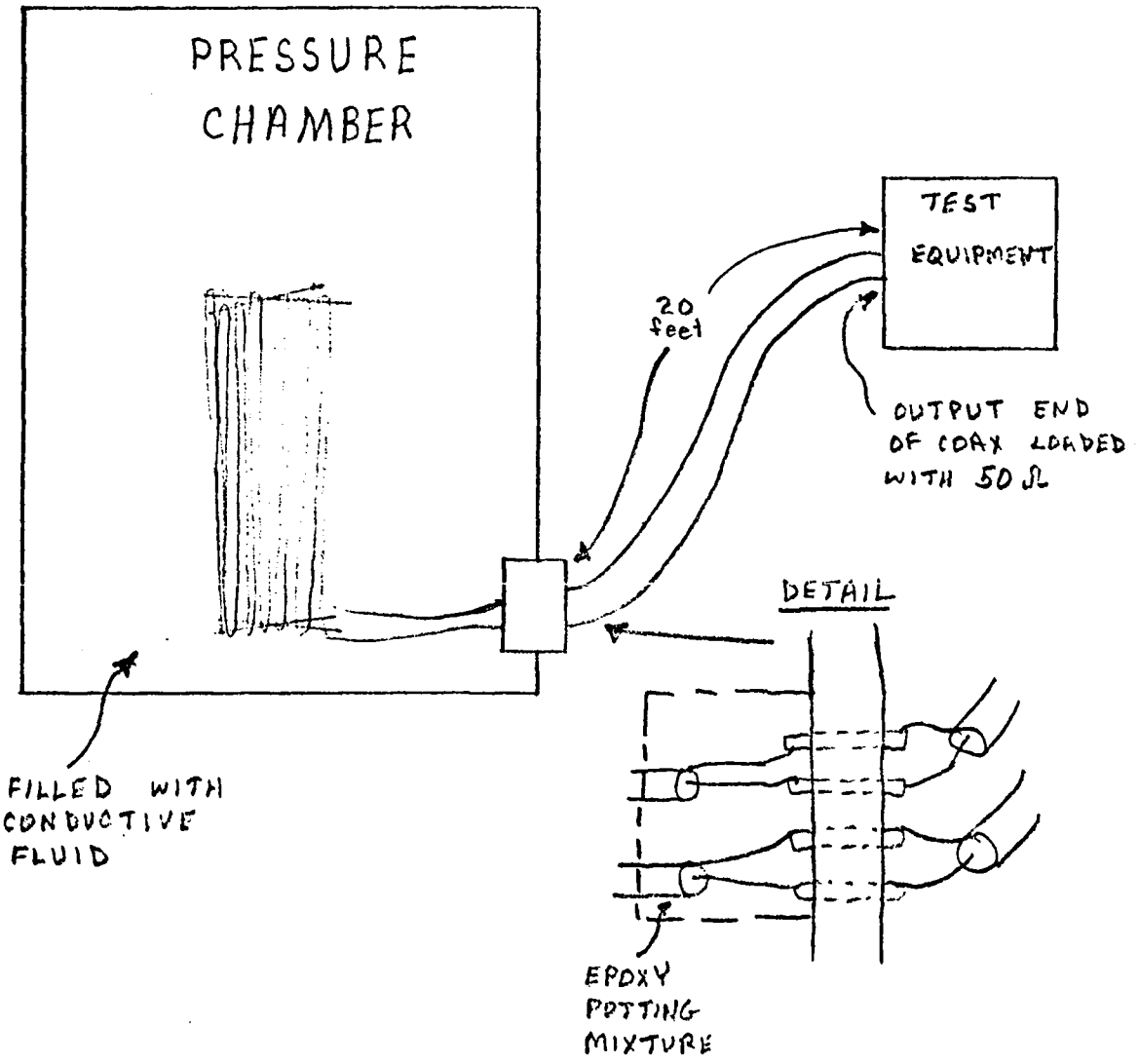
C. For Insulation Resistance:

Freed 1620 Megohmeter

NOTE: For low value insulation resistances a Simpson VDM or HP34705A/ HP34703A were used and are noted on the data sheets.

3.0 TEST DATA

A completed set of data sheets from Memo HRS-75-014 is attached. The original is on file at Bendix.



TEST SET-UP

FIGURE 1

Table 1 contains the data from these data sheets. For easier interpretation the data were plotted for the six pressure cycles (see Figures 2, 3, and 4).

4.0 CONCLUSIONS

Except for the insulation resistance between the coax shield and the conductive fluid, the test results were positive indications that the coax can be used in a pressure environment. The long term effects of a salt water environment on the cable should be investigated before the cable is put into service.

Table 2 contains the average values and standard deviation for the entire set of data.

		PRETEST	10K PSI	AMBIENT	10K PSI	AMBIENT	10K PSI	AMBIENT	10K PSI	AMBIENT	10K PSI	AMBIENT	10K PSI	AMBIENT
ATTENUATION db	50KHZ	2.3	2.4	2.2	2.3	2.4	2.4	2.4	2.3	2.4	2.3	2.3	2.3	2.3
	500KHZ	2.75	2.8	2.8	2.8	2.7	2.7	2.8	2.6	2.7	2.6	2.7	2.7	2.7
	1MHZ	4.5	4.5	4.5	4.5	4.5	4.5	4.5	4.5	4.5	4.4	4.5	4.4	4.4
	1.5MHZ	5.3	5.8	5.5	5.8	5.5	5.8	5.4	5.7	5.4	5.8	5.6	5.7	5.5
	3MHZ	7.9	8.7	8.2	8.7	8.2	8.7	8.2	8.5	8.2	8.7	8.2	8.6	8.2
	6MHZ	10.4	8.8	9.2	8.5	9.5	8.8	9.4	9.4	9.7	9.4	9.6	9.0	9.3
INSULATION RESISTANCE	CENT/SHLD KMΩ	1.20	1.44	1.80	1.68	2.40	2.64	3.36	2.40	2.80	2.40	2.80	2.88	2.80
	SHLD/FLUID MΩ	3	2	2	5.1	3	5.2	.6	.035	.09	100	3	65	.3
DC RESISTANCE Ω	CENT COND	10.63	10.72	10.60	10.73	10.60	10.70	10.58	10.69	10.56	10.70	10.58	10.69	10.58
	SHLD	4.49	4.42	4.46	4.46	4.46	4.47	4.47	4.42	4.44	4.43	4.44	4.44	4.47

TEST DATA
TABLE 1

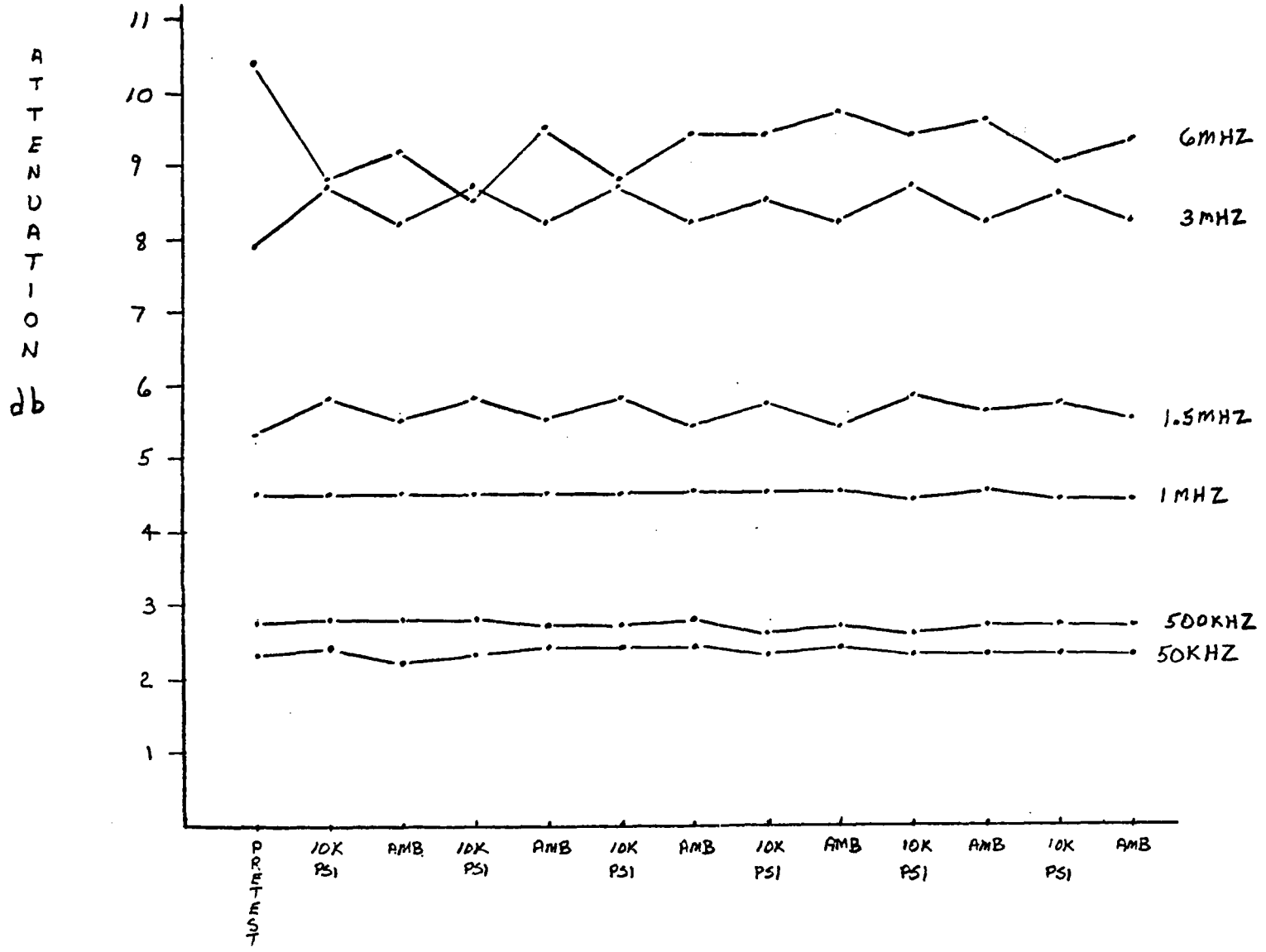

ATTENUATION db
11
10
9
8
7
6
5
4
3
2
1
6MHZ
3MHZ
1.5MHZ
1MHZ
500KHZ
50KHZ
PRETEST
10K PSI
AMB
10K PSI
AMB
10K PSI
AMB
10K PSI
AMB
10K PSI
AMB
10K PSI
AMB

FIGURE 2

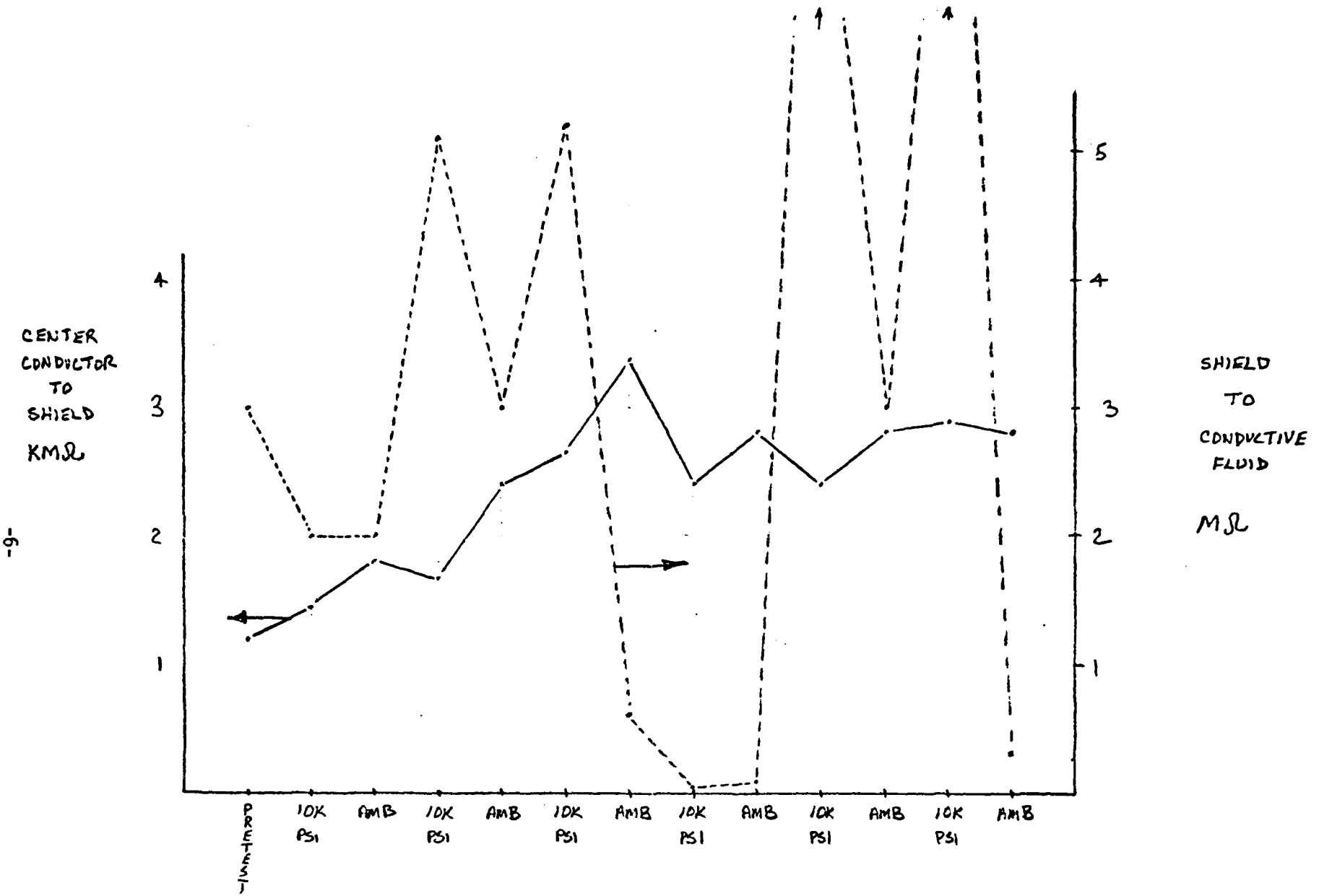


FIGURE 3
INSULATION RESISTANCE

Average $\bar{x} = \dfrac{\sum_{i=1}^{13} x_i}{13}$

Standard Deviation $S = \sqrt{\dfrac{\sum_{i=1}^{13} x_i^2 - \dfrac{\left(\sum_{i=1}^{13} x_i\right)^2}{13}}{12}}$

		$\bar{x}$	S
Attenvation	50KHZ	2.33 db	.063
	500KHZ	2.72 db	.069
	1MHZ	4.48 db	.044
	1.5MHZ	5.60 db	.178
	3MHZ	8.38 db	.273
	6MHZ	9.31 db	.480
Insulation Resistance	CENT/SHLD	2.35 KMΩ	.639
	SHLD/FLUID	14.56 MΩ	31.033
DC Resistance	SHLD	4.45 Ω	.022
	CENT. COND.	10.643 Ω	.063

TABLE 2

TEST DATA DISTRIBUTION

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HRS-75-014
25 April 1975

TEST PLAN COAX PRESSURE TEST

1. OBJECT

The object of the test is to evaluate the effects of high pressure on the electrical performance of RG58U coaxial cable.

2. PRESSURE CYCLES

The pressure will be cycled six times from sea level to 10000 psi and back to sea level. The pressure will be held one hour at 10000 psi. The cable will be in a conductive fluid.

3. ELECTRICAL MEASUREMENTS

The following electrical measurements are to be made at each stop at sea level and at the end of each one hour hold at 10000 psi.

A. Attenuation At:

50 kHz
500 kHz
1 MHz
1.5 MHz
3 MHz
6 MHz

B. Insulation resistance at 600 Vdc from center conductor to shield and shield to conductive fluid.

c. DC resistance of shield and center conductor.

4. RECORDED DATA

Data shall be recorded as follows:

A. Initial Data Date: _____

Chamber Temperature: 61 °F

Measured cable length: 1000 ft.

Attenuation at 50 kHz: 2.30 db

500 kHz: 2.75

4. Recorded Data Contd.

A. Initial data contd.

Attenuation at 1 MHz:	4.5 db
1.5 MHz:	5.3
3 MHz:	7.9
6 MHz:	10.4
Insulation Res. cent. cond/ shield	1.2 KMΩ
Shield/fluid	≈3MΩ (simpson)
DC Res. shield	4.49 Ω
DC center cond.	10.63 Ω

B. First Cycle

Pressure start time:	9:20
Time at 10000 psi:	9:50
Time of measurements:	10:50
Chamber temperature:	61°F
Atten. at 50 kHz:	2.4
500 kHz:	2.8
1 MHz:	4.5
1.5 MHz:	5.8
3 MHz:	8.7
6 MHz:	8.8
Insul. Res. cent. cond/shield:	1.44 KMΩ
shield/fluid:	≈2MΩ (simpson)
DC Res. shield:	4.42
center cond.	10.72

4. Recorded Data Contd.

B. First Cycle contd.

Start depressure time:	11:11
Time of measurements:	11:16
Atten. at 50 kHz:	2.2 db
500 kHz:	2.8
1 MHz:	4.5
1.5 MHz:	5.5
3 MHz:	8.2
6 MHz:	9.2
Insul. Res. cent. cond/shield:	1.80 KMΩ
shield/fluid:	2MΩ (simpson)
DC Res. shield:	4.46 Ω
center cond.	10.60 Ω

C. Second Cycle

Pressure start time:	11:25
Time at 10000 psi:	11:55
Time of measurements:	13:00
Chamber temperature:	61°F
Atten. at 50 kHz:	2.3 db
500 kHz:	2.8
1 MHz:	4.5
1.5 MHz:	5.8
3 MHz:	8.7
6 MHz:	8.5

4. Recorded Data Contd.

C. Second cycle contd.

Insul. Res. cent. cond/shield:	1.68 KMΩ
Shield/fluid:	5.1 MΩ (HP34703A)
DC Res. shield:	4.46 Ω
Center cond.	10.73 Ω
Start depressure time:	13:20
Time of measurements:	13:26
Atten. at 50 kHz:	2.4 db
500 kHz:	2.7
1 MHz:	4.5
1.5 MHz:	5.5
3 MHz:	8.2
6 MHz:	9.5
Insul. Res. cent. cond/shield:	2.4 KMΩ
Insul. Res. shield/fluid:	3 MΩ (HP34703A)
DC Res. shield:	4.46 Ω
DC Res. center cond.	10.6 Ω

D. Third Cycle

Pressure start time:	13:36
Time at 10000 psi:	14:00
Time of measurements:	15:05
Chamber temperature:	61°F
Atten. at 50 kHz:	2.4 db
500 kHz:	2.7
1 MHz:	4.5
1.5 MHz:	5.8

4. Recorded Data Contd.

D. Third cycle contd.

Atten. at 3 MHz:	8.7 db
6 MHz:	8.8
Insul. Res. cent. cond/shield:	2.64 KMΩ
Shield/fluid:	5.2 MΩ (HP34703A)
DC Res. shield:	4.47 Ω
DC res. center cond.:	10.7 Ω
Start depressure time:	15:15
Time of measurements:	15:21
Atten. at 50 kHz:	2.4 db
500 kHz:	2.8
1 MHz:	4.5
1.5 MHz:	5.4
3 MHz:	8.2
6 MHz:	9.4
Insul. Res. cent. cond/shield:	3.36 KMΩ
Insul. Res. shield/fluid:	600KΩ (HP34703A)
DC res. shield:	4.47 Ω
DC res. center cond.	10.58 Ω

E. Fourth Cycle

Pressure start time:	8:04
Time at 10000 psi:	8:32
Time of measurements:	9:32
Chamber temperature:	61°F

4. Recorded Data Contd.

E. Fourth cycle contd.

Atten. at 50 kHz:	2.3 db
500 kHz:	3.6
1 MHz:	4.5
1.5 MHz:	5.7
3 MHz:	8.5
6 MHz:	9.4
Insul. Res. cent. cond/shield:	2.4 KMΩ
Insul. Shield/fluid:	35 KΩ (simpson)
DC Res. shield:	4.42 Ω
DC Res. center cond.:	10.69 Ω
Start depressure time:	9:45
Time of measurements:	9:51
Atten. at 50 kHz:	2.4 db
500 kHz:	2.7
1 MHz:	4.5
1.5 MHz:	5.4
3 MHz:	8.2
6 MHz:	9.7
Insul. Res. cent. cond/shield:	2.8 KMΩ
Insul. Res. shield/fluid:	90 KΩ (simpson)
DC Res. shield:	4.44
DC Res. center cond.:	10.56

4. Recorded Data Contd.

F. Fifth Cycle

Pressure start time:	10:05
Time at 10000 psi:	10:32
Time of measurements:	11:32
Chamber temperature:	61°F
Atten. at 50 kHz:	2.3 db
500 kHz:	2.6
1 MHz:	4.4
1.5 MHz:	5.8
3 MHz:	8.7
6 MHz:	9.4
Insul. Res. cent. cond/shield:	2.4 KMΩ
Insul Res. shield/fluid:	100 MΩ @ 50v
DC Res. shield:	4.43 Ω
DC Res. center cond.:	10.70 Ω
Start depressure time:	11:43
Time of measurements:	11:48
Atten. at 50 kHz:	2.3 db
500 kHz:	2.7
1 MHz:	4.5
1.5 MHz:	5.6
3 MHz:	8.2
6 MHz:	9.6

4. Recorded Data Contd.

F. Fifth cycle contd.

Insul. Res. cent. cond/shield: 2.8 KMΩ

Insul. Res. shield/fluid: 3 MΩ @50v

DC Res. shield: 4.44 Ω

DC Res. center cond.: 10.58 Ω

G. Sixth Cycle

Pressure start time: 11:59

Time at 10000 psi: 12:24

Time of measurements: 13:33

Chamber temperature: 61°F

Atten. at 50 kHz: 2.3 db

500 kHz: 2.7

1 MHz: 4.4

1.5 MHz: 5.7

3 MHz: 8.6

6 MHz: 9.0

Insul. Res. cent. cond/shield: 2.88 KMΩ

Insul. Res. shield/fluid: 65 MΩ @50v.

DC Res. shield: 4.44 Ω

DC Res. center cond.: 10.69 Ω

Start depressure time: 13:48

Time of measurements: 13:58

4. Recorded Data Contd.

G. Sixth cycle contd.

Atten. at 50 kHz:	2.3 db
500 kHz:	2.7
1 MHz:	4.4
1.5 MHz:	5.5
3 MHz:	8.2
6 MHz:	9.3
Insul. Res. cent. cond/shield:	2.8 KMΩ
Insul. Res. shield/fluid:	300 KΩ (simpson)
DC Res. shield:	4.47 Ω
DC Res. center cond.:	10.58 Ω

After the test the pressure chamber was half emptied and ≈ 8 feet of cable were cut from each end of the cable. The feed-thru connections were then measured as below:

Insulation resistance input/fluid 850 MΩ
" " output/fluid 350 MΩ